SIEMENS

SIMATIC

S7-400
S7-400 Automation System, CPU Specifications

Manual

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Safety Guidelines

This manual contains notices you have to observe in order to ensure your personal safety, as well as to prevent damage to property. The notices referring to your personal safety are highlighted in the manual by a safety alert symbol, notices referring only to property damage have no safety alert symbol. These notices shown below are graded according to the degree of danger.

Danger

indicates that death or severe personal injury **will** result if proper precautions are not taken.

Warning

indicates that death or severe personal injury **may** result if proper precautions are not taken.

Caution

with a safety alert symbol, indicates that minor personal injury can result if proper precautions are not taken.

Caution

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Introduction

1

Purpose of the manual

The information contained in this manual can be used as a reference for operating, for descriptions of the functions, and for the technical specifications of the CPUs of the S7-400.

How to configure, assemble and wire these and further modules in an S7-400 system is described in the *S7-400 Programmable Controller; Hardware and Installation* manual for each system.

Basic Knowledge Required

To understand this manual, you should have general experience in the field of automation engineering.

You should also have experience of working with computers or PC-type tools (for example programming devices) and the Windows operating system 2000 or XP. Since the S7-400 is configured with the STEP 7 basic software, you should also have experience of working with the basic software. You can acquire this knowledge in the manual *Programming with STEP 7*.

In particular when using an S7-400 in areas subject to safety regulations, note the information relating to the safety of electronic controllers in the Appendix of the manual *S7-400 Programmable Controller; Hardware and Installation* manual.

Range of Validity of This Manual

The manual is valid for the S7-400 automation system. It applies to the CPUs listed below:

- CPU 414-3 PN/DP; (6ES7414-3EM05-0AB0)
- CPU 416-3 PN/DP; (6ES7416-3ER05-0AB0)
- CPU 416-3F PN/DP; (6ES7416-3FR05-0AB0)

General Technical Data

You will find information about certificates, approvals and standards in the manual *S7-400 Programmable Controller; Module Specifications*.

Related Documentation

This manual is part of the documentation package for S7-400.

System	Documentation package
S7-400	• S7-400 Automation System; Hardware and Installation • S7-400 Automation Systems; Module Specifications • Instruction List S7-400 • S7-400 Automation System; CPU Specifications

Orientation

The manual contains various features that allow you to find specific information more quickly:

- At the start of the manual you will find a complete table of contents and a list of the diagrams and tables that appear in the manual.
- Finally, a comprehensive index allows quick access to information on specific subjects.

Recycling and Disposal

The S7-400 is low in contaminants and can therefore be recycled. Contact a certified electronic-waste disposal company for information and help on environmentally-friendly recycling and disposal of your old equipment.

Further Assistance

Please talk to your Siemens contact at one of our representatives or local offices if you have questions about the products described here and do not find the answers in this manual.

You will find information on who to contact at:

http://www.siemens.com/automation/partner

A signpost to the documentation of the various SIMATIC products and systems is available at:

http://www.siemens.com/simatic-tech-doku-portal

The online catalog and online ordering system is available at:

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Training Center

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- Information about on-site services, repairs and spare parts. You will find much more under "Services."

Structure of a CPU 41x

2

2.1 Control and display elements of the CPUs

Control and Display Elements of the CPU 41x-3PN/DP

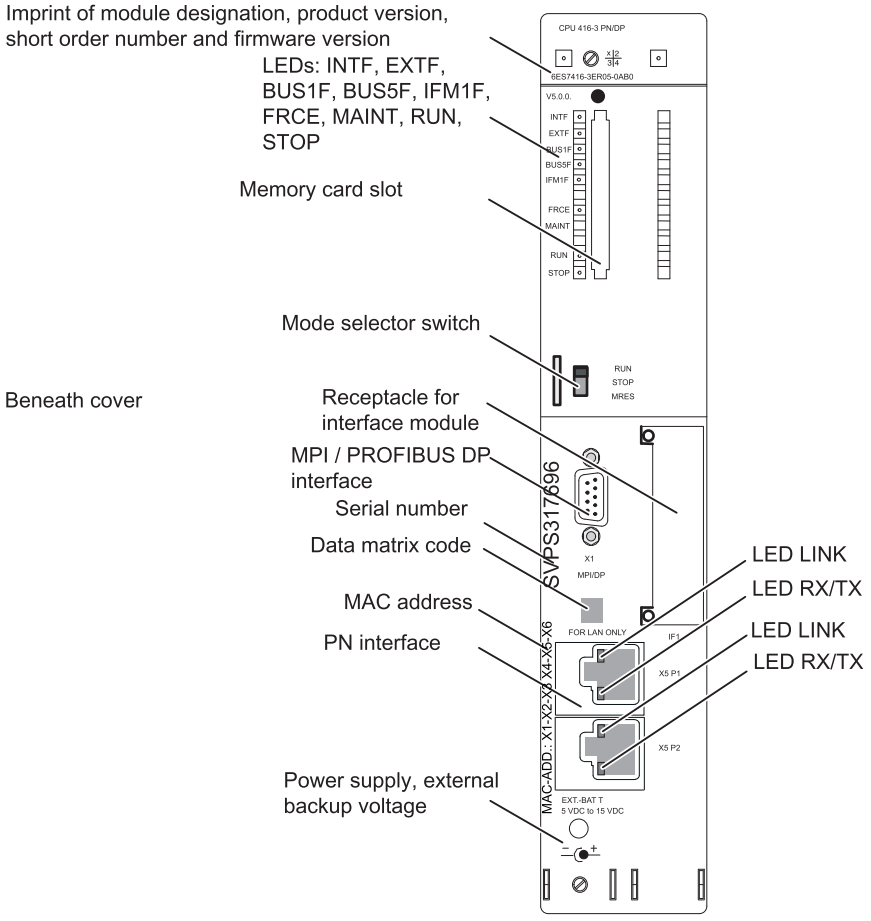


Figure 2-1 Location of the Control and Display Elements of the CPU 41x-3PN/DP

LEDs

The table below gives you an overview of the LEDs on the individual CPUs.

Table 2-1 LEDs of the CPUs

LED	Color	Meaning	Exists on CPU
			414-3 PN/DP 416-3 PN/DP 416F-3 PN/DP
INTF	Red	Internal fault	x
EXTF	Red	External fault	x
FRCE	Yellow	Force job active	x
MAINT		Not assigned	x
RUN	Green	RUN mode	x
STOP	Yellow	STOP mode	x
BUS1F	Red	Bus fault on MPI/PROFIBUS DP interface 1	x
BUS5F	Red	Features of the PROFINET interface	x
IFM1F	Red	Fault on interface module 1	x

Mode Selector Switch

You can use the mode selector switch to set the current mode of the CPU. The mode selector is a three-position toggle switch.

Memory Card Slot

You can insert a memory card into this slot.

There are two types of memory cards:

- RAM cards

  You can expand CPU load memory with the RAM card.

- Flash cards

  The flash card is non-volatile storage for storing your user program and data (no backup battery necessary). You can program the flash card either on the programming device or in the CPU. The flash card also expands the load memory of the CPU.

Slot for Interface Modules

You can insert one PROFIBUS DP module for the CPU 41x-3 and CPU 41x-4 in this slot.

MPI/DP Interface

You can connect various devices to the MPI interface of the CPU, for example:

- Programming devices
- Operator control and monitoring devices
- Other S7-400 or S7-300 controllers

Use the bus connection connector with oblique cable outlet, see the manual *S7-400 Automation System, Hardware and Installation*.

You can also configure the MPI interface as a DP master so that you can use it as PROFIBUS DP interface with up to 32 DP slaves.

PROFIBUS DP Interface

You can connect the distributed I/O, programming devices/OPs and other DP master stations to the PROFIBUS DP interface.

PROFINET Interface

You can connect PROFINET IO devices to the PROFINET interface. The PROFINET interface has 2 RJ 45 sockets and is equipped with a 2-port switch. The PROFINET interface provides the connection to the Industrial Ethernet, CBA, etc..

Caution

You can only connect to a LAN with this interface. You cannot connect to the public telecommunication network.

Power Supply, External Backup Voltage at the "EXT.-BATT." Jack

You can install either one or two backup batteries in the S7-400 power supply modules, depending on the module type to achieve the following:

- You back up the user program stored in RAM.
- You retain the values of flags, timers, counters, system data and the data in dynamic DBs.
- You back up the internal clock.

You can achieve the same backup by supplying a voltage between 5 V DC and 15 V DC to the "EXT.-BATT." jack of the CPU.

The "EXT.-BATT." input has the following features:

- Polarity reversal protection
- Short-circuit current limited to 20 mA

You need a cable with a 2.5 mm Ø jack plug to connect the power supply to the "EXT.-BATT" jack, as shown in the following illustration. Make sure the polarity of the jack plug is correct.

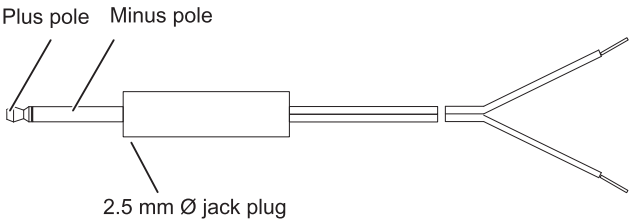


Figure 2-2 Connecting Cable with Jack Plug

You can order a jack plug with an assembled cable from the Electronic Plant Karlsruhe under the order number A5E00728552A.

Note

You require the external power supply to the "EXT.-BATT." jack when you replace a power supply module and want to backup the user program stored in RAM and the data mentioned above while you are replacing the module.

See also

Monitoring functions of the CPU (Page 2-5)

Status and error displays (Page 2-8)

Multipoint Interface (MPI) (Page 2-21)

2.2 Monitoring functions of the CPU

Monitoring Functions and Error Messages

The CPU hardware and the operating system monitoring functions ensure proper functioning of the system and a defined reaction to faults and errors. Certain error events also trigger a reaction in the user program. When recursive errors occur, the LED is switched off with the next incoming error.

The table below provides an overview of possible errors, their causes and the reactions of the CPU.

Table 2-2 Faults/Errors and the reactions of the CPU

Type of error	Cause of error	Response of the operating system	Fault LED
Access error (entering state)	Module failure (SM, FM, CP) I/O read access error I/O write access error	The "EXTF" LED stays lit until the error is acknowledged. With SMs: • OB 122 call • Entry in the diagnostic buffer • With input modules: "NULL" entered as data in the accumulator or the process image With other modules: • OB 122 call If the OB is not loaded: The CPU changes to STOP	EXTF
Timeout error (entering state)	• The user program execution time (OB1 and all interrupt and error OBs) exceeds the specified maximum cycle time. • OB request error • Overflow of the startup information buffer • Watchdog interrupt • Resume RUN after CiR	The "INTF" LED is lit until the error is acknowledged. OB 80 call If the OB is not loaded: The CPU changes to STOP	INTF
Faulty power supply module(s), (not mains failure), (entering and exiting state)	In the central or expansion rack • At least one backup battery of the power supply module is exhausted • Backup voltage is missing • The 24 V DC supply of the power supply module has failed	OB 81 call If the OB is not loaded: The CPU remains in RUN.	EXTF

Type of error	Cause of error	Response of the operating system	Fault LED
Diagnostic interrupt (entering and exiting state)	An I/O module with interrupt capability reports a diagnostic interrupt	OB 82 call If the OB is not loaded: The CPU changes to STOP	EXTF
Remove/insert module interrupt (entering and exiting state)	Removal or insertion of an SM and insertion of the wrong module type. The LED EXTF does not light up if only one SM is installed and then removed while the CPU is in STOP (default setting). The LED lights up briefly when the SM is inserted again.	OB 83 call If the OB is not loaded: The CPU changes to STOP	EXTF
CPU Hardware error (entering state)	• A memory error was detected and eliminated	OB 84 call If the OB is not loaded: The CPU remains in RUN.	INTF
Priority class error (Only entering state, depending on OB85 mode)	• A priority class is called, but the corresponding OB is not present. • In the case of an SFB call: The instance DB is missing or bad. • Error while updating the process image	OB 85 call If the OB is not loaded: The CPU changes to STOP	INTF EXTF
Rack / station failure (entering and exiting state)	• Power failure on an expansion module • PROFINET DP chain failure • PROFINET IO subsystem failure • Failure of a coupling chain: missing or defective IM, cable break)	OB 86 call If the OB is not loaded: The CPU changes to STOP	EXTF
Communication error (entering state)	• Unable to enter status information in the DB (shared data communication) • Incorrect message frame (shared data communication) • Incorrect message length (shared data communication) • Error in the structure of the shared data frame (shared data communication) • DB access error	OB 87 call	INTF

Type of error	Cause of error	Response of the operating system	Fault LED
Execution abort (entering state)	• Synchronous error nesting depth exceeded • Too many nested block calls (B stack) • Error when allocating local data	OB 88 call If the OB is not loaded: The CPU changes to STOP	INTF
Programming error (entering state)	Errors in the user program • BCD conversion error • Range length error • Range error • Alignment error • Write error • Timer number error • Counter number error • Block number error • Block not loaded	OB 121 call If the OB is not loaded: The CPU changes to STOP	INTF
Code error (entering state)	Error in the compiled user program (for example, illegal OP code or a jump beyond block end)	The CPU changes to STOP Restart or CPU memory reset required.	INTF
Loss of the clock signal (entering state)	When using isochronous mode: Clock pulses were lost either because OB61 ... 64 was not started due to higher priorities, or because additional asynchronous bus loads suppressed the bus clock pulses.	OB 80 call If the OB is not loaded: The CPU changes to STOP Call of OB 61..64 at the next pulse.	INTF

Further test and information functions are available in each CPU and you can invoke these in STEP 7.

2.3 Status and error displays

Status LEDs

The RUN and STOP LEDs on the front panel of the CPU indicate the current CPU mode.

Table 2-3 Possible states of the RUN and STOP LEDs

LED		Meaning
RUN	STOP	
H	D	CPU is in RUN.
D	H	CPU is in STOP. The user program is not executed. Cold restart, restart and warm restart/reboot is possible. If STOP was triggered by an error, the error LED (INTF or EXTF) is also set.
B 2 Hz	B 2 Hz	CPU is in DEFECTIVE status. The INTF, EXTF, FRCE, BUSF1, BUSF5 and IFM1F LEDs also flash.
B 0.5 Hz	H	CPU HOLD was triggered by a test function.
B 2 Hz	H	A warm restart / cold restart / hot restart was triggered. It can take a minute or longer to execute these functions, depending on the length of the OB called. If the CPU still does not change to RUN, there may be an error in the system configuration.
x	B 0.5 Hz	The CPU requests memory reset.
x	B 2 Hz	Memory reset in progress or the CPU is currently being initialized following POWER ON.
D = LED is dark; H = LED is lit; B = LED flashes at the specified frequency; x = LED status is irrelevant		

Error and Fault Displays and Special Characteristics

The three LEDs INTF, EXTF and FRCE on the front panel of the CPU indicate errors and special features in user program execution.

Table 2-4 Possible statuses of the INTF, EXTF and FRCE LEDs

LED			Meaning
INTF	EXTF	FRCE	
H	x	x	An internal error was detected (programming or parameter assignment error) or the CPU is performing a CiR.
x	H	x	An external error was detected (in other words, the cause of the error is not on the CPU module).
x	x	H	A force job is active.
x	x	B 2 Hz	Node flash test function.
H = LED is lit; B = LED flashes with the specified frequency; x = LED status is irrelevant			

The LEDs BUS1F and BUS5F indicate errors on the MPI/DP, PROFIBUS DP and PROFINET IO interfaces.

Table 2-5 Possible states of the BUS1F and BUS5F LEDs

LED		Meaning	
BUS1F	BUS5F		
H	x	An error was detected on the MPI/DP interface.	
x	x	An error was detected on the PROFIBUS DP interface.	
x	H	An error was detected on the PROFINET IO interface.	
B	x	CPU is DP master:	One of more slaves on the PROFIBUS DP interface are not responding.
		CPU is DP slave:	CPU is not addressed by the DP master.
H = LED is lit; B = LED flashes; x = LED status is irrelevant			

Error and Fault Displays and Special Characteristics

The CPUs 41x-3 also feature the IFM1F LED. This LED indicates problems relating to the memory submodule interface.

Table 2-6 Possible states of the IFM1F LED

LED	Meaning	
IFM1F		
H	An error was detected on memory submodule interface.	
B	CPU is DP master:	One of more slaves on the PROFIBUS DP interface module inserted in the receptacle are not responding.
	CPU is DP slave:	CPU is not addressed by the DP master.
H = LED is lit; B = LED flashes; x = LED status is irrelevant		

Error and Fault Displays and Special Characteristics of the CPU 41x-3PN/DP

The CPUs 41x-3PN/DP furthermore have the LINK LED and the RX/TX LED These LEDs indicate the current state of the PROFINET interface.

Table 2-7 Possible states of the LINK and RX/TX LEDs

LED		Meaning
LINK	RX/TX	
H	x	Connection at PROFINET interface is active
x	B 6 Hz	Receive / transmit data at the PROFINET interface.
H = LED is lit; B = LED flashes with the specified frequency; x = LED status is irrelevant		

Note

Note

The LINK and RX/TX LEDs are located directly at the sockets of the PROFINET interface. They are not labeled.

LED MAINT

This LED currently has no function.

Diagnostic Buffer

In STEP 7, you can select "PLC -> Module status" to read the cause of an error from the diagnostic buffer.

2.4 Mode selector switch

Function of the Mode Selector Switch

You can use the mode selector to set the CPU from RUN to STOP or reset CPU memory. STEP 7 offers further mode selection options.

Positions

The mode selector is designed as a toggle switch. The following figure shows all positions of the mode selector.

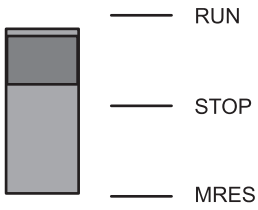


Figure 2-3 Mode selector switch settings

The following table explains the settings of the mode selector switch. In the event of a fault or if there are problems preventing a startup, the CPU goes into STOP or retain this mode, regardless of the position of the mode selector switch.

Table 2-8 Mode selector switch settings

Position	Notes
RUN	If there is no startup problem or error and the CPU was able to go into RUN, the CPU either executes the user program or remains idle. Access to the I/O is possible. • You can upload programs from the CPU to the programming device (CPU -> Programming device) • You can upload programs from the programming device to the CPU (Programming device -> CPU).
STOP	The CPU does not execute the user program. The digital signal modules are locked. The output modules are disabled in the default parameter configuration. • You can upload programs from the CPU to the programming device (CPU -> Programming device) • You can upload programs from the programming device to the CPU (Programming device -> CPU).
MRES (CPU memory reset; master reset)	Momentary-contact position of the toggle switch for CPU memory reset (see next pages).

Security Classes

A security class can be agreed for S7-400 CPUs in order to prevent unauthorized access to CPU programs. You can define a security class which allows users access to PG functions

without particular authorization (password). On password level you can access all PG functions.

Setting the Security Classes

You can set the security classes (1 to 3) for a CPU in STEP 7 -> HW Config.

You can delete the security class set STEP 7 -> HW Config by means of a manual reset using the mode selector switch.

The following table lists the security classes of an S7-400 CPU.

Table 2-9 Security classes of an S7-400 CPU

CPU function	Protection level 1	Protection level 2	Protection level 3
Display of the block list	Access allowed	Access allowed	Access allowed
Monitoring Variables	Access allowed	Access allowed	Access allowed
STACKS module status	Access allowed	Access allowed	Access allowed
Operator control and monitoring functions	Access allowed	Access allowed	Access allowed
S7 communication	Access allowed	Access allowed	Access allowed
Read time of day	Access allowed	Access allowed	Access allowed
Set Time of Day	Access allowed	Access allowed	Access allowed
Block status	Access allowed	Access allowed	Password required
Downloading to the programming device	Access allowed	Access allowed	Password required
Downloading to the CPU	Access allowed	Password required	Password required
Delete blocks	Access allowed	Password required	Password required
Memory compression	Access allowed	Password required	Password required
Download user program to memory card	Access allowed	Password required	Password required
Control selection	Access allowed	Password required	Password required
Control variable	Access allowed	Password required	Password required
Breakpoints	Access allowed	Password required	Password required
Leave hold	Access allowed	Password required	Password required
Memory reset	Access allowed	Password required	Password required
Force	Access allowed	Password required	Password required

2.5 Running a memory reset

Operating Sequence at Memory Reset

Case A: You want to transfer a new, complete user program to the CPU.

1. Set the mode selector switch to STOP.

   Result: The STOP LED is lit.

2. Set the selector to MRES and hold it there.

   Result: The STOP LED is switched off for one second, on for one second, off for one second and then remains on.

3. Turn the switch back to the STOP setting, then to the MRES setting again within the next 3 seconds, and back to STOP.

   Result: The STOP LED flashes for at least 3 seconds at 2 Hz (memory being reset) and then remains lit.

Running a Memory Reset following a Request

Case B: The CPU requests memory reset, indicated by the flashing STOP LED at 0.5 Hz.
The system requests a CPU memory reset, for example, after a memory card was removed or inserted.

1. Set the mode selector switch to MRES and then back to STOP.

   Result: The STOP LED flashes for at least 3 seconds at 2 Hz (memory being reset) and then remains lit.

For detailed information on CPU memory reset refer to the manual *S7-400 Automation System, Hardware and Installation*.

What happens in the CPU during a memory reset

When you run a memory reset, the following process occurs on the CPU:

- The CPU deletes the entire user program from main memory and load memory (integrated RAM and, if applicable, RAM card).
- The CPU clears all counters, bit memory, and timers (except for the time of day).
- The CPU tests its hardware.
- The CPU initializes its hardware and system program parameters (internal default settings in the CPU). Some default settings selected by the user will be taken into account.
- If a flash card is inserted, the CPU copies the user program and the system parameters stored on the flash card into main memory after the memory reset.

Values Retained After a Memory Reset

After the CPU has been reset, the following values remain:

- The content of the diagnostic buffer

  The content can be read out with the programming device using STEP 7.
- Parameters of the MPI (MPI address and highest MPI address). Note the special features shown in the table below.
- The IP address of the CPU
- The subnet mask
- The SNMP parameters
- The time of day
- The status and value of the operating hours counter

Special Features MPI parameters and IP address

A special situation is presented for the MPI parameters and IP address when a CPU memory reset is preformed. The following table shows which MPI parameters and IP address remain valid after a CPU memory reset.

Table 2-10 MPI parameters and IP address following memory reset

Memory reset ..	MPI parameters and IP address ...
With inserted FLASH card	..., stored on the FLASH card are valid
Without plugged FLASH card	...are retained in the CPU and valid

2.6 Cold start / Warm restart / Hot restart

Cold start

- During a cold restart, all data (process image, bit memory, timers, counters and data blocks) are reset to the start values stored in the program (load memory), irrespective of whether they were configured as retentive or non-retentive.
- Corresponding startup OB is OB 102
- Program execution is restarted at the beginning (OB 102 or OB 1).

Restart (Warm Restart)

- A warm restart resets the process image and the non-retentive flags, timers, times and counters.

  Retentive flags, times and counters retain their last valid value.

  All data blocks assigned the "Non Retain" attribute are reset to the load values. The remaining data blocks retain their last valid value.
- Corresponding startup OB is OB 100
- Program execution is restarted at the beginning (OB 100 or OB 1).
- After a power supply interruption, the warm restart function is only available in backup mode.

Hot Restart

- When a hot restart is performed, all data and the process image retain their last valid value.
- Program execution is resumed at the breakpoint.
- The outputs do not change their status until the current cycle is completed.
- Corresponding startup OB is OB 101
- After a power supply interruption, the hot restart function is only available in backup mode.

Operating Sequence at Restart (Warm Restart)

1. Set the mode selector to STOP.

   Result: The STOP LED is lit.
2. Set the switch to RUN.

Whether the CPU executes a warm restart or hot restart depends on the CPU parameter settings.

Operating Sequence at Hot Restart

1. Select the startup type "hot restart" on the PG

   The button is active only if this type of startup is possible on the specific CPU.

Operating Sequence at Cold Start

A manual cold restart can only be triggered on the programming device.

2.7 Structure and Functions of the Memory Cards

Order numbers

The order numbers for memory cards are listed in the technical specifications.

Structure

The memory card is slightly larger than a credit card and protected by a strong metal casing. It is inserted into a front slot of the CPU. The memory card casing is encoded to allow only one position of insertion.

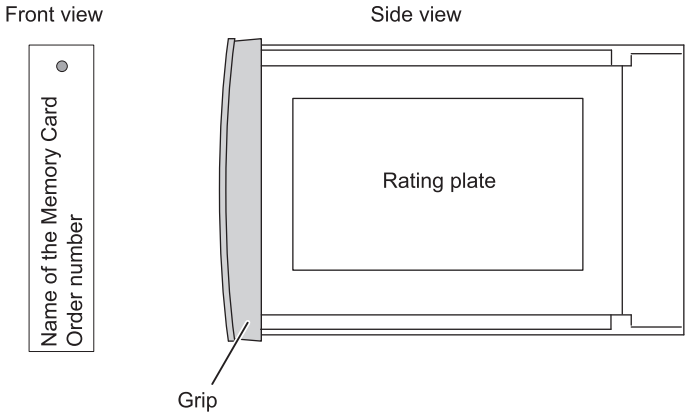


Figure 2-4 Structure of the Memory Card

Function

The memory card and an integrated memory area on the CPU together form the load memory of the CPU. During runtime, the load memory contains the complete user program including comments, symbols and special additional information that allows the decompilation of the user program, and all module parameters.

What Is Stored in the Memory Card

The following data can be stored on memory cards:

- User program, in other words, blocks (OBs, FBs, FCs, DBs) and system data
- Parameters which determine the behavior of the CPU
- Parameters which determine the behavior of the I/O modules.
- In STEP 7 V5.1 or higher, all project data on suitable Memory Cards.

Serial Number

As from Version 5 the memory cards have a serial number. This serial number is listed in INDEX 8 of the SZL Parts List W#16#xy1C. The parts list can be read out using the SFC 51 "RDSYSST".

You can determine the following when you read the serial number into your user program: The user program can only be started when a specific memory card is inserted in the CPU. This protects against unauthorized copying of the user program, similar to a dongle.

See also

Overview of the memory concept of S7-400 CPUs (Page 8-1)

2.8 Use of the Memory Cards

Types of Memory Cards for S7-400

Two types of memory card are used in the S7-400:

- RAM cards
- Flash cards (FEPROM cards)

Note

Parameters which determine the behavior of the CPU Non-Siemens memory cards cannot be used in the S7-400.

Which Type of Memory Card Should Be Used?

Whether you use a RAM card or a flash card depends on how you intend to use the memory card.

Table 2-11 Types of Memory Cards

If you ...	Then ...
Want to store the data in RAM and edit your program in RUN,	Use a **RAM card**
Want to store your user program permanently on the memory card, even with power removed (without backup or outside the CPU),	Use a **Flash card**

RAM card

To use a RAM card and load the user program, you must insert it into the CPU slot. The user program is loaded with the help of the programming device (PG).

You can load the entire user program or individual elements such as FBs, FCs, OBs, DBs, or SDBs to the load memory in when the CPU is in STOP mode or RUN.

All data on the RAM Card are lost when you remove it from the CPU. The RAM card does not have a built-in backup battery.

If the power supply has a functioning backup battery or an external backup voltage is supplied to the CPU via the "EXT. BATT." socket, the contents of the RAM card are retained after power is switched off, provided the RAM card stays in the CPU and the CPU stays in the rack.

Flash Card

You have two options of loading the user program when using a flash card:

Option 1:

1. Set the CPU mode switch to the STOP state with the mode selector switch.
2. Insert the flash card into the CPU.
3. Perform a memory reset.
4. Load the user program with the STEP 7 command "PLC -> Download User Program to Memory Card".

Option 2:

1. Load the user program to the flash card when the programming device / programming adapter is offline.
2. Insert the flash card into the CPU.

You can only reload the full user program using the Flash card. You can load smaller program sections into the integrated load memory on the CPU using the programming device. In the case of extensive program changes, you must always reload the Flash card with the full user program.

The Flash card does not require a backup voltage, that is, the information stored on it is retained even when you remove the Flash card from the CPU or if you operate your S7-400 system without a buffering function (without backup battery in the power supply module or "EXT. BATT." socket of the CPU).

Which Memory Card Capacity Should Be Used?

The capacity of the required memory card is based on the size of the user program and amount of system data.

To optimize utilization of work memory (code and data) on your CPU, you should expand the load memory of the CPU with a memory card which has at least the same capacity as the work memory.

Changing the Memory Card

To change the memory card:

1. Set the CPU to STOP.
2. Remove the memory card.

Note

If you remove the memory card, the CPU requests a memory reset in a 3-sec sequence, which is indicated by the flashing STOP LED. This sequence cannot be influenced by error OBs.

3. Insert the "new" memory card in the CPU.
4. Reset the CPU memory.

2.9 Multipoint Interface (MPI)

Availability

All the CPUs of the S7-400 feature an MPI interface.

Connectable Devices

You can connect the following stations to the MPI, for example:

- Programming devices (PG/PC)
- Control and monitoring devices (OPs and TDs)
- Additional SIMATIC S7 PLCs

Some devices use the 24 VDC power supply of the interface. This voltage is provided at the MPI interface connected to a reference potential

Programming Device/OP ->CPU Communication

A CPU is capable of maintaining several simultaneous online connections. Only one of these connections is reserved as default connection for a programming device, and a second for the OP/ control and monitoring device.

For CPU-specific information on the number of connection resources of connectable OPs, refer to the Technical Specifications.

Time synchronization By Using MPI

Time synchronization is possible by using the MPI interface of the CPU. The CPU can be master or slave.

CPU-CPU Communication

There are three types of CPU-CPU communication:

- Data transfer by means of S7 basic communication
- Data transfer by means of S7 communication
- Data transfer by means of global data communication

For further information, refer to the *Programming with STEP 7* manual.

Connectors

Always use bus connectors with the oblique cable outlet for PROFIBUS DP or PG cables used to connect devices to the MPI (see the manual *S7-400 Automation System, Hardware and Installation*).

MPI interface as a PROFIBUS DP interface

You can also configure the MPI interface for operation as a PROFIBUS DP interface. To do so, you can reconfigure the MPI interface under STEP 7 in HW Config. You can use this to set up a DP line consisting of up to 32 slaves.

Reference

You can find information about planning time synchronization in the manual *Process Control System PCS7; Safety Concept*.

2.10 PROFIBUS DP Interface

Availability

CPUs with a "PN" name suffix are equipped with a PROFINET DP interface as a plug-in module. To be able to use this interface, you must first configure it in HW Config and then load the configuration in the CPU.

Connectable Devices

The PROFIBUS DP interface is used to build up a PROFIBUS master system or to connect PROFIBUS IO devices.

You can connect any compliant DP slave to the PROFIBUS DP interface.

Here, the CPU is operated either as a DP master or a DP slave which is connected via PROFIBUS DP field bus to the passive slave stations or other DP masters.

Some devices use the 24 VDC power supply of the interface. This voltage is provided at the PROFIBUS DP interface connected to a reference potential.

Connectors

Always use the bus connector for PROFIBUS DP or PROFIBUS cables used to connect devices to the PROFIBUS DP interface (see the manual *S7-400 Automation System, Hardware and Installation*).

Time synchronization Using PROFIBUS

As the time master, the CPU sends synchronization message frames to the PROFIBUS to synchronize further stations.

As the time slave, the CPU receives the CPU synchronization message frames from other time masters. One of the following devices can be a time master:

- A CPU 41x with internal PROFIBUS interface
- A CPU 41x with external PROFIBUS interface, for example CP 443-5
- A PC with a CP 5613 or CP 5614

Reference

You can find information about planning time synchronization in the manual *Process Control System PCS7; Safety Concept*.

2.11 PROFINET (PN) interface

Availability

CPUs with a "PN" name suffix feature an ETHERNET interface with PROFINET functionality.

Assigning an IP Address

You have the following options to assign an IP address to the Ethernet interface:

1. With the SIMATIC Manager command "PLC -> Edit Ethernet Node".
2. With the CPU properties in HW Config. Then download the configuration to the CPU.

Devices Capable of PROFINET (PN) Communication

- Programming device/PC with Ethernet network card and TCP protocol
- Active network components (Scalance X200, for example)
- S7-300 / S7-400 with Ethernet CP (for example, CPU 416-2 with CP 443-1)
- PROFINET IO devices (for example, IM 151-3 PN in an ET 200S)
- PROFINET CBA components

Connectors

Use only 2 x RJ45 connectors (2-port switch) to connect devices to the PROFINET interface.

Time Synchronization Using PROFINET

Time synchronization in the NTP procedure The CPU is an NTP client in this case.

Reference

- For instructions on how to configure the integrated PROFINET interface, refer to the manual *S7-400 Automation System, Hardware and Installation*.
- For further information on PROFINET, refer to *PROFINET System Description*
- For detailed information about Ethernet networks, network configuration and network components refer to the *SIMATIC NET Manual: Twisted-Pair and Fiber Optic Networks*, available under article ID 8763736 at http://support.automation.siemens.com.
- *Component Based Automation, Commissioning SIMATIC iMap Systems - Tutorial,* Article ID 18403908
- Further information about PROFINET: http://www.profinet.com

2.12 Overview of the parameters for the S7-400 CPUs

Default Values

When shipped all parameters are set to default values. These defaults are suitable for a whole range of standard applications, in other words, an S7-400 can be used immediately without requiring any further settings.

You can define CPU-specific default values using the "HW Config" tool in STEP 7.

Parameter Fields

The behavior and properties of the CPU are specified in the parameters that are stored in system data blocks. The CPUs have a defined initial default status. You can modify this default status by changing the parameters in HW Config.

The list below provides an overview of the selectable system properties of the CPUs.

- General properties, for example, the CPU name
- Startup, for example, enabling hot restarts
- Synchronous cycle interrupts
- Cycle/clock memory (e.g. scan cycle monitoring time)
- Retentivity, meaning the number of flags, timers and counters that are retained during a restart
- Memory, for example local data

  Note: If you change the work memory allocation by modifying parameters, this work memory is reorganized when you load system data to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

  The usable size of the working memory for logic or data blocks is changed when loading the system data if you change the following parameters:

  – Size of the process image, byte-oriented; in the "Cycle/Clock Memory" tab
  – Communication resources in the "Memory" tab
  – Size of the diagnostic buffer in the "Diagnostics/Clock" tab
  – Number of local data for all priority classes in the "Memory" tab

- Assignment of interrupts, hardware interrupts, time-delay interrupts and asynchronous error interrupts to the priority classes
- Time-of-day interrupts, for example start, interval duration and priority
- Cyclic interrupts, for example priority, interval duration
- Diagnostics/clock, for example time-of-day synchronization
- Protection levels
- Web

Note

16 memory bytes and 8 counters are set to retentive in the default settings, in other words, they are not deleted when the CPU is restarted.

Parameter Assignment Tool

You can set the individual CPU parameters using "Hardware Configuration" in STEP 7.

Note

If you make changes to the existing settings of the following parameters, the operating system initializes the same setting as for a cold restart.

- Size of the process image of the inputs
- Size of the process image of the outputs
- Size of the local data
- Number of diagnostic buffer entries
- Communication resources

This involves the following initializations:

– Data blocks are initialized with the load values.

– Memory bits, timers, counters, inputs and outputs are deleted regardless of the retentivity setting (0).

– DBs generated by SFC are deleted

– Permanently configured, base communication connections are terminated

– All run levels are initialized.

Special functions of a CPU 41x

3

3.1 Web Server

Reading Out Information About the Web Server

The web server can be used to read the following information out of the CPU:

- Start page with general CPU information
  - Module name
  - Module type
  - Hardware order number
  - Hardware release version
  - Firmware release version
  - Plant identifier
  - Mode
  - Status
  - Mode selector switch setting
- Contents of the diagnostics buffer
- Messages (message state ALARM_S, ALARM_SQ, ALARM_D, ALARM_DQ) without acknowledgement possibility
- Information about Industrial Ethernet
  - Ethernet MAC address
  - IP address
  - IP subnet address
  - Default router
  - Auto Negotiation Mode ON/OFF
  - Number of packages sent/received
  - Number of faulty packages sent/received
  - 10 Mbps or 100 Mbps full duplex
  - Link status

Activating Web Server

The web server is activated in its factory state. It is deactivated in HW Config with its basic configuration. You can activate the web server in HW Config with the command "CPU -> Object Properties -> Web".

Web Access on the CPU

Proceed as follows to access the web server:

1. Connect the programming device/PC via the Ethernet interface with the CPU.
2. Open the Web browser (for example, the Internet Explorer).

Enter the IP address of the CPU in the "Address" field of the web browser in the form http://a.b.c.d.
The start page of the CPU opens. From the start page you can navigate to further information.

You can also access the web server using a PDA. Use the address format http:\\a.b.c.d/basic for this access.

Display Languages

You can select 2 of the following 5 languages for the display of the alarm texts and of the diagnostic buffer. However, you can only select the languages in which you have installed STEP 7.

- German
- English
- French
- Spanish
- Italian

Selecting Display Languages

Select the display languages in HW Config under "CPU -> Object Properties -> Web".

If you configure message texts for the message blocks AlarmS/SQ and AlarmD/DQ, you have to compile the HW Config again afterwards.

Safety

The web server by itself does not provide any security. Protect your web-compatible CPUs against unauthorized access by means of a firewall.

Timeliness of the Display

The information displayed by the web server is static, in other words, the display is not updated. However, you can see the most recent data when you print out the information.

3.2 Multicomputing

3.2.1 Fundamentals

Multicomputing Mode

Multicomputing mode is the simultaneous operation of several (maximum 4) CPUs with Multicomputing capability in a central controller of the S7-400.

The CPUs involved automatically change their modes synchronized with each other; the CPUs start up together and change to STOP together. The user program on each CPU runs independently of the user programs on the other CPUs. This allows control tasks to be performed simultaneously.

Racks Suitable for Multicomputing

The following racks are suitable for multicomputing:

- UR1 and UR2
- UR2-H, multicomputing with several CPUs is possible only if the CPUs are in the same subdevice.
- CR3, since the CR3 has only 4 slots, multicomputing is possible only with two CPUs.

Difference Compared with Operation in a Segmented Rack

In the CR2 segmented rack (physically segmented, cannot be set using parameters), only one CPU per segment is permitted. This is, however, not multicomputing. The CPUs in the segmented rack each form an independent subsystem and behave like individual processors. There is no common logical address space.

Multicomputing is not possible in the segmented rack (see also *S7-400 Automation System, Hardware and Installation*).

Uses

There are benefits in using multicomputing in the following situations:

- When your user program is too large for one CPU and memory starts running short, distribute your program on several CPUs.
- When a particular part of your plant needs to be processed quickly, separate the relevant program section from the overall program and run this part on a separate "fast" CPU.
- When your plant consists of several parts with a clear demarcation between them so that they can be controlled relatively independently, process plant part 1 on CPU1, plant part 2 on CPU2 etc.

Example

The following figure shows an automation system operating in multicomputing mode. Each CPU can access the modules assigned to it (FM, CP, SM).

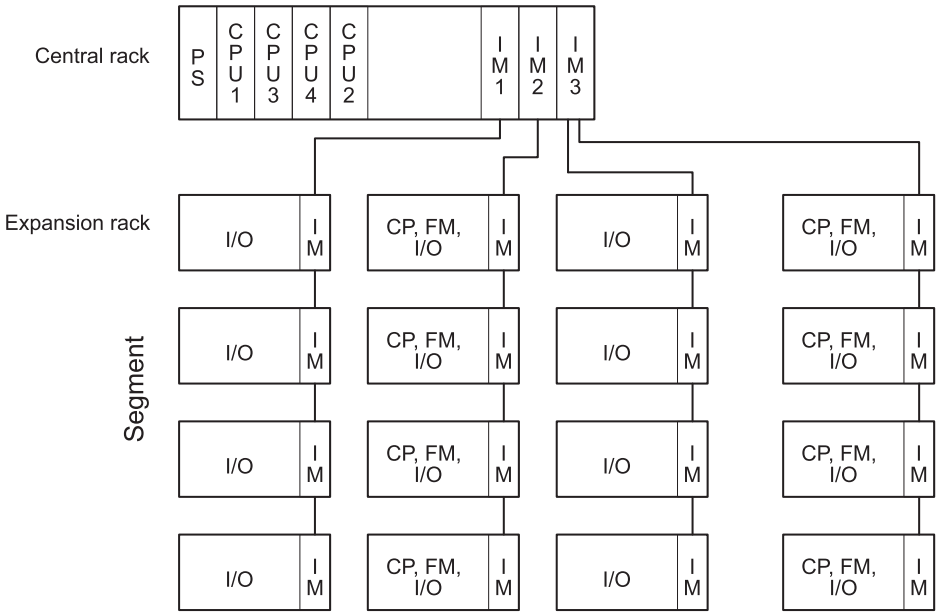


Figure 3-1 Example of multicomputing

3.2.2 Special Features at Multicomputing

Slot Rules

In multicomputing mode, up to four CPUs can be inserted in one central controller (CC) in any order.

Bus Connection

All the CPUs can be reached from the programming device if a corresponding configuration exists by means of the MPI interface or the PROFIBUS DP interface.

Behavior during Startup and Operation

During startup, the CPUs involved in multicomputing automatically check whether they can synchronize themselves. Synchronization is possible only in the following situations:

- When all the configured and only the configured CPUs are inserted and ready to operate.
- When correct configuration data were created with STEP 7 and were downloaded to the plugged CPUs.

If one of these conditions is not met, the event with ID 0x49A4 is entered in the diagnostic buffer. You will find explanations of the event IDs in the reference help on standard and system functions.

When exiting the STOP mode, there is a comparison of the types of startup COLD RESTART/WARM RESTART/HOT RESTART. If the types of startup are different, the CPUs do **not** change to RUN.

Address and Interrupt Assignment

In multicomputing, the individual CPUs can access the modules assigned to them during configuration with STEP 7. The address area of a module is always assigned "exclusively" to one CPU.

In particular, this means that every module with interrupt capability is assigned to a CPU. Interrupts triggered by such a module cannot be received by the other CPUs.

Interrupt Processing

The following applies to interrupt processing:

- Hardware interrupts and diagnostic interrupts are sent to only one CPU.
- If a module fails or is removed/inserted, the interrupt is processed by the CPU to which the module was assigned during parameter assignment with STEP 7.
  Exception: A remove/insert interrupt triggered by a CP reaches all CPUs even if the CP was assigned to one CPU during configuration with STEP 7.
- If a rack fails, OB86 is called on every CPU; in other words, it is also called on the CPUs to which no module in the failed rack was assigned.

For more detailed information on OB86, refer to the reference help on organization blocks.

Number of I/Os

The number of I/Os of an automation system in multicomputing mode corresponds to the number of I/Os of the CPU with the most resources. The configuration limits for the specific CPU or specific DP master must not be exceeded in the individual CPUs.

3.2.3 Multicomputing interrupt

Principle

Using the multicomputing interrupt (OB60), you can synchronize the CPUs involved in multicomputing to an event. In contrast to the hardware interrupts that are triggered by signal modules, the multicomputing interrupt can only be output by CPUs. The multicomputing interrupt is triggered by calling SFC35 "MP_ALM".

For more detailed information, refer to the *System Software for S7-300/400, System and Standard Functions*.

3.2.4 Configuring and programming multicomputing mode

Reference

For information on the procedure for configuring and programming CPUs and modules, refer to the *Configuring Hardware and Connections with STEP 7*.

3.3 System modifications during operation

3.3.1 Basics

Overview

The option of making system changes using CiR (Configuration in RUN), makes it possible to implement certain configuration changes in RUN. Processing of the process is held for a short period of time. The upper limit of this period of time is set to 1 s as default but can be changed by the user. During this time, process inputs retain their last value (see also *"Modifying the System during Operation via CiR"* manual).

You can download this manual free of charge from the Internet at the following address:
`http://www.siemens.com/automation/service&support`

System modifications during operation with CiR can be made in plant sections with distributed I/O. Such changes are only possible with the configuration as shown in the figure below. To ensure clarity, we assume a single DP master system and a single PA master system. These restrictions do not, however, exist in reality.

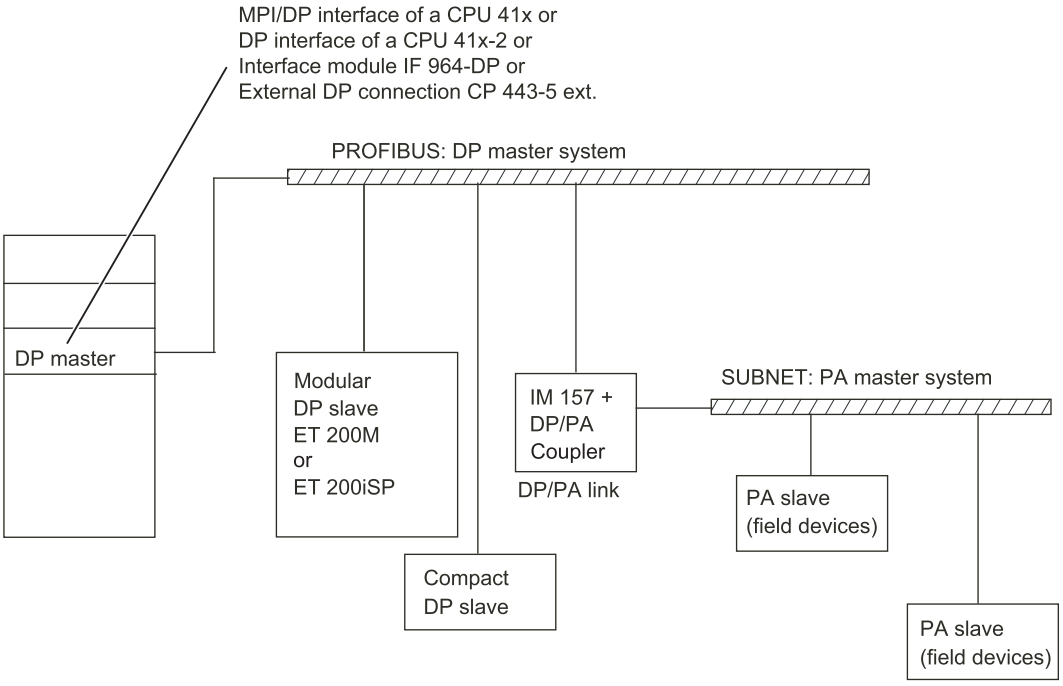


Figure 3-2 Overview: System structure for system modifications during operation

3.3.2 Hardware requirements

Hardware requirements for system modifications during operation

To be able to make system modifications during operation, the following hardware requirements must be met during commissioning:

- If you want to make system changes to a DP master system with an external DP master (CP 443-5 extended) during operation, this must have at least firmware version V5.0.
- If you want to add modules to an ET 200M: Use of the IM 153-2 as of MLFB 6ES7153-2BA00-0XB0 or the IM 153-2FO as of MLFB 6ES7 153-2BB00-0XB0. You must also set up the ET 200M with active bus elements and adequate free space for the planned expansion. The ET 200M must not be linked as a DPV0 slave (using a GSD file).
- If you want to add entire stations: Reserve the necessary bus connectors, repeaters etc.
- If you want to add PA slaves (field devices): Use of the IM 157 as of MLFB 6ES7157-0AA82-0XA00 in the appropriate DP/PA-Link.
- Use of the CR2 rack is not permitted.
- The use of one or more of the modules listed below within a station in which you want to make system changes during operation with CiR is not permitted. CP 444, IM 467.
- No multicomputing
- No isochronous operation in the same DP master system

Note

You can mix components that are compliant with system changes during operation and those that are not (with the exception of the modules excluded above). You can, however, only make modifications to CiR-compliant components.

3.3.3 Software requirements

Software Requirements for System Modifications during Operation

To be able to make configuration changes in RUN, the user program must meet the following requirement: It must be written so that, for example, station failures, module faults or timeouts do not cause the CPU to change to STOP.

The following OBs must be available on your CPU:

- Hardware interrupt OBs (OB 40 to OB 47)
- Time jump OB (OB80)
- Diagnostic interrupt OB (OB82)
- Remove/insert OB (OB83)
- CPU hardware fault OB (OB84)
- Program execution error OB (OB85)
- Rack failure OB (OB86)
- I/O access error OB (OB122)

3.3.4 Permitted system modifications

Overview

During operation, you can make the following system modifications:

- Add modules to the ET 200M modular DP slave provided that you have not linked it as a DPV0 slave (using a GSD file).
- Change the parameter assignment of ET 200M modules, for example, setting different limits or using previously unused channels.
- Use previously unused channels in a module or submodule in the ET 200M, ET 200S, ET 200iS modular slaves.
- Add DP slaves to an existing DP master system.
- Add PA slaves (field devices) to an existing PA master system.
- Add DP/PA couplers downstream from an IM157.
- Add PA-Links (including PA master systems) to an existing DP master system.
- Assign added modules to a process image partition.
- Reassign parameters for existing ET 200M stations (standard modules and fail-safe signal modules in standard mode).
- Reversing changes: Added modules, submodules, DP slaves and PA slaves (field devices) can be removed again.

Note

If you want to add or remove slaves or modules or modify the existing process image partition assignment, this is possible in a maximum of four DP master systems.

All other modifications not specifically permitted above are not permitted during operation and are not discussed further here.

3.4 Resetting the CPU to the factory state

Factory state of the CPU

A memory reset is performed when you reset the CPU to its factory state and the properties of the CPU are set to the following values:

Table 3-1 Properties of the CPU in the factory state

Properties	Value
MPI address	2
MPI transmission rate	187.5 Kbps
Contents of the diagnostics buffer	Empty
IP parameters	None
Operating hours counters	o
Date and time	01.01.94, 00:00:00

Procedure

Proceed as follows in order to reset a CPU to the factory state:

1. Switch off the supply voltage.
2. If a memory card is inserted in the CPU, always remove the memory card.
3. Hold the toggle switch in the MRES setting and switch the supply voltage on again.
4. Wait until LED pattern 1 from the subsequent overview is displayed.
5. Release the toggle switch, set it back to MRES within 3 seconds and hold it in this position.
   After approx. 4 seconds all the LEDs light up.
6. Wait until LED pattern 2 from the subsequent overview is displayed.
   This LED pattern lights up for approximately 5 seconds. During this period you can abort the resetting procedure by releasing the toggle switch.
7. Wait until the LED pattern 3 from the subsequent overview is displayed and release the toggle switch again.

The CPU is now reset to the factory state. It starts without buffering and changes to the STOP mode. The event "Reset to factory setting" is entered in the diagnostic buffer.

LED Patterns during CPU Reset

While you are resetting the CPU to the factory state, the LEDs light up consecutively in the following LED patterns:

Table 3-2 LED patterns

LED	LED pattern 1	LED pattern 2	LED pattern 3
INTF	F 0.5 Hz	F 0.5 Hz	H
EXTF	D	D	D
BUSxF	D	D	D
FORCE	F 0.5 Hz	D	D
IFMxF	D	D	D
RUN	F 0.5 Hz	D	D
STOP	F 0.5 Hz	D	D
D = LED is dark; L = LED lights up; F = LED flashing with the specified frequency			

3.5 Updating firmware online

Basic Procedure

To update the firmware of a CPU, you receive the four files (*.UPD) containing the current firmware. Load these files in the CPU. You do not need a memory card to perform an online update.

Requirement

The CPU whose firmware you want to update must be available online, for example, via Profibus, MPI or Industrial Ethernet. The files containing the current firmware version must be available in the PG/PC file system. A folder may contain only the files of one firmware version.

Note

Use Industrial Ethernet if possible to update the firmware of your CPU. Depending on the configured transmission rate, updating via MPI or DP may take considerably more time.

Procedure

Proceed as follows to update the firmware of a CPU:

1. Open the station containing the CPU you want to update.
2. Select the CPU.
3. Select the menu command "PLC > Update Firmware".
4. In the "Update Firmware" dialog, select the path to the firmware update files (*.UPD) using the "Browse" button.

   After you selected a file, the information in the lower fields of the "Update Firmware" dialog box shows you the modules for which the file is suited and the specific firmware version.
5. Click "Run."

STEP 7 verifies that the selected file can be interpreted by the CPU and then downloads the file to the CPU. If this requires changing the operating state of the CPU, you will be asked to perform these tasks in the relevant dialog boxes.

3.6 Reading out service data

Requirement

To use this function, you must install STEP 7, version 5.3 or higher.

Use Case

In a service situation in which you need to call Customer Support, it is possible that Customer Support will need special information about the status of a CPU in your system for diagnostic purposes. This information is stored in the diagnostic buffer and in the actual service data.

You can read this information with the menu command "PLC > Save Service Data" and save it in two files. You can then send this to Customer Support.

Note the following:

- Save the service data directly after a CPU changes to STOP mode if possible.

You specify the path and the file name under which the service data are stored are specified when the information is the read.

Procedure

1. Select the respective CPU with the menu command "SIMATIC Manager > Accessible Nodes".
2. Select the menu command "PLC > Save Service Data".

   A dialog box opens in which you specify the storage location and name of the two files.
3. Save the file.
4. If requested, send the files to Customer Support.

Communication

4

4.1 interfaces

4.1.1 Multi-Point Interface (MPI)

Availability

The MPI/DP interface of an S7-400 CPU in the factory state is set as an MPI interface with an address of 2.

Properties

The MPI represents the CPU interface for PG/OP connections or for communication on an MPI subnet.

The preset transmission rate for all CPUs is 187.5 Kbps. The maximum transmission rate is 12 Mbps.

The CPU automatically broadcasts its configured bus parameters via the MPI interface (the baud rate, for example). A programming device, for example, can thus receive the correct parameters and automatically connect to a MPI subnet.

Note

In runtime, you may only connect programming devices to an MPI subnet.
Other stations, such as OP or TP, should not be connected to the MPI subnet in runtime. Otherwise, transferred data might be corrupted due to interference pulses or global data packages may be lost.

Time synchronization

Time synchronization is possible by using the MPI interface of the CPU. The CPU can be master or slave.

MPI Interface as a PROFIBUS DP Interface

You can also configure the MPI interface for operation as a PROFIBUS DP interface. To do so, you can reconfigure the MPI interface under STEP 7 in HW Config. You can use this to set up a DP line consisting of up to 32 slaves.

Devices capable of MPI communication

- PG/PC
- OP/TP
- S7-300 / S7-400 with MPI interface
- S7-200 only with 19.2 Kbps and 187.5 Kbps

4.1.2 PROFIBUS DP

Availability

CPUs with a "PN" name suffix are equipped with a PROFINET DP interface as a plug-in module. To be able to use this interface, you must first configure it HW Config and then load the configuration in the CPU.

A CPU with MPI/DP interface is supplied with a default MPI configuration. You need to set DP mode in STEP 7 if you want to use the DP interface.

Properties

The PROFIBUS DP interface is mainly used to connect distributed I/O. You can configure the PROFIBUS DP interface as master or slave. It allows a transmission rate of up to 12 Mbps.

The CPU broadcasts its bus parameters, such as the transmission rate, via the PROFIBUS DP interface when master mode is set. A programming device, for example, can thus receive the correct parameters and automatically connect to a PROFIBUS subnet.

Note

For DP interface in slave mode only

When you disable the Commissioning / Debug mode / Routing check box in the DP interface properties dialog in STEP 7, all user-specific transmission rate settings will be ignored, and the transmission rate of the master is automatically set instead. This disables the routing function at this interface.

Time synchronization via PROFIBUS DP

As the time master, the CPU sends synchronization message frames to the PROFIBUS to synchronize further stations.

As the time slave, the CPU receives the CPU synchronization message frames from other time masters. One of the following devices can be a time master:

- A CPU 41x with internal PROFIBUS interface
- A CPU 41x with external PROFIBUS interface, for example CP 443-5
- A PC with a CP 5613 or CP 5614

Devices capable of PROFIBUS DP communication

The PROFIBUS DP interface is used to build up a PROFIBUS master system or to connect PROFIBUS IO devices.

The following devices can be connected to the PROFIBUS DP interface:

- PG/PC
- OP/TP
- PROFIBUS DP slaves
- PROFIBUS DP master

Here, the CPU is operated either as a DP master or a DP slave which is connected via PROFIBUS DP field bus to the passive slave stations or other DP masters.

Some devices use the 24 VDC power supply of the interface. This voltage is provided at the PROFIBUS DP interface connected to a reference potential.

Reference

Further information on PROFIBUS: http://www.profibus.com

4.1.3 PROFINET

Availability

CPUs with a "PN" name suffix feature an ETHERNET interface with PROFINET functionality.

Assigning an IP Address

You have the following options to assign an IP address to the Ethernet interface:

1. With the SIMATIC Manager command "PLC -> Edit Ethernet Node".
2. With the CPU properties in HW Config. Then download the configuration to the CPU.

Devices Capable of PROFINET (PN) Communication

- Programming device/PC with Ethernet network card and TCP protocol
- Active network components (Scalance X200, for example)
- S7-300 / S7-400 with Ethernet CP (for example, CPU 416-2 with CP 443-1)
- PROFINET IO devices (for example, IM 151-3 PN in an ET 200S)
- PROFINET CBA components

Connectors

Use only 2 x RJ45 connectors (2-port switch) to connect devices to the PROFINET interface.

Properties of the PROFINET Interface

Properties and protocols
PROFINET IO PROFINET CBA
IEC61784-2 , Conformance Class A, B and C
Open block communication via • TCP ISO • UDP • ISO on TCP • S7 communication Programming device functions
SNMP
Time synchronization in the NTP procedure

Properties	
Connector design	2 x RJ45
	Switch with 2 ports Switch with Store and Forward procedures
Transmission speed	Max. 10/100 Mbps
	Autosensing Autocrossing Autonegotiation
Media	Twisted Pair Cat5

Note

Networking PROFINET Components

Full duplex mode with 100 Mbps is mandatory for PROFINET IO.

Reference

- For further information on PROFINET, refer to *PROFINET System Description*
- For detailed information about Ethernet networks, network configuration and network components refer to the *SIMATIC NET Manual: Twisted-Pair and Fiber Optic Networks*, available under article ID 8763736 at http://support.automation.siemens.com.
- *Component Based Automation, Commissioning SIMATIC iMap Systems - Tutorial,* Article ID 18403908

Further information about PROFINET: http://www.profinet.com

4.2 Communication services

4.2.1 Overview of communication services

Overview

Table 4-1 Communication services of the CPUs

Communication service	Functionality	Assignment of S7 connection resources	via MPI	via DP	via PN/IE
Programming device communication	Commissioning, test, diagnostics	Yes	X	X	X
OP communication	Operator control and process monitoring	Yes	X	X	X
S7 basic communication	Data exchange	Yes	X	–	–
S7 communication	Data exchange in server and client mode: Configuration of communication required.	Yes	Only in server mode	Only in server mode	X
Global data communication	Cyclic data communication (for example, flag bits)	No	X	–	–
Routing PG functions	for example testing, diagnostics across networks	Yes	X	X	X
PROFIBUS DP	Data communication between master and slave	No	–	X	–
PROFINET CBA	Data communication by means of component based communication	No	–	–	X
PROFINET IO	Data communication between IO controllers and the IO devices	No	–	–	X
Web server	Diagnostics	No	–	–	X
SNMP (Simple Network Management Protocol)	Standard protocol for network diagnostics and configuration	No	–	–	X
Open communication by means of TCP/IP	Data exchange via Industrial Ethernet with TCP/IP protocol (with loadable FBs)	Yes	–	–	X
Open communication by means of ISO on TCP	Data exchange via Industrial Ethernet with ISO-on-TCP protocol (with loadable FBs)	Yes	–	–	X
Open communication by means of UDP	Data communication via Industrial Ethernet with UDP protocol (with loadable FBs)	Yes	–	–	X

Connection resources In the S7-400

The components of the S7-400 have a number of connection resources depending on the module.

4.2.2 PG communication

Properties

Programming device communication is used to exchange data between engineering stations (PG, PC, for example) and SIMATIC modules which are capable of communication. This service is available for MPI, PROFIBUS and Industrial Ethernet subnets. Routing between subnets is also supported.

You can use the programming device communication for the following actions:

- Loading programs and configuration data
- Performing tests
- Evaluating diagnostic information

These functions are integrated in the operating system of SIMATIC S7 modules.

A CPU can maintain several simultaneous online connections to one or multiple programming devices.

4.2.3 OP communication

Properties

OP communication is used to exchange data between HMI stations, such as WinCC, OP, TP and SIMATIC modules which are capable of communication. This service is available for MPI, PROFIBUS and Industrial Ethernet subnets.

You can use the OP communication for operator control, monitoring and alarms. These functions are integrated in the operating system of SIMATIC S7 modules. A CPU can maintain several simultaneous connections to one or several OPs.

4.2.4 S7 basic communication

Properties

S7-based communication is used to exchange data between S7 CPUs and the communication-capable SIMATIC modules within an S7 station (acknowledged data communication). The service is available via MPI subnet, or within the station to function modules (FM).

You do not need to configure connections for basic S7 communication. The integrated communication functions are called via SFCs in the user program.

SFCs for the Basic S7 Communication

The following SFCs are integrated in the operating system of the S7-400 CPUs:

Table 4-2 SFCs for the Basic S7 Communication

Block	Block name	Brief description
SFCs for external communication		
SFC 65 SFC 66	X_SEND X_RCV	Secure transmission of a data block to the communication partner.
SFC 67	X_GET	Reading variables from a communication partner
SFC 68	X_PUT	Writing variables to a communication partner
SFC 69	X_ABORT	Cancellation of an established connection with transmission of data
SFCs for internal communication		
SFC 72	I_GET	Reading variables from a communication partner
SFC 73	I_PUT	Writing variables to a communication partner
SFC 74	I_ABORT	Cancellation of an established connection with transmission of data

Reference

- Refer to the *operation list* to learn which SFCs are included in the operating system of a CPU.
- You can find detailed descriptions of the SFCs in the *STEP 7 Online Help* or *System and Standard Functions* reference manual.

4.2.5 S7 communication

Properties

A CPU can always operate as a server or client in S7 communication: A connection is configured permanently. The following connections are:

- One-sided configured connections (for PUT/GET only)
- Two-side configured connections (for USEND, URCV, BSEND, BRCV, PUT, GET)

S7-400 PN CPUs provide an integrated Industrial Ethernet port on the CPU module, allowing you to use S7 communication over Industrial Ethernet without going through a communications processor (CP). Use a CP 443 for S7 communication for other S7-CPUs.

The S7-400 features integrated S7 communication services that allow the user program in the controller to initiate reading and writing of data. The S7 communication functions are called via SFBs in the user program. These functions are independent of the specific network, allowing you to program S7 communication over PROFINET, Industrial Ethernet, PROFIBUS, or MPI.

S7 communication services provide the following features:

- During system configuration, you configure the connections used by the S7 communication. These connections remain configured until you download a new configuration.
- You can establish several connections to the same partner. The number of communication partners accessible at any time is restricted to the number of connection resources available.

S7 communication allows you to transfer a block of up to 64 KB per call to the SFB. An S7-400 transfers a maximum of 4 variables per block call.

SFBs for the Basic S7 Communication

The following SFBs are integrated in the operating system of the S7-400 CPUs:

Table 4-3 SFBs for the basic S7 communication

Block	Block name	Brief description
SFB 8 SFB 9	USEND URCV	Send data to a remote partner SFB with the type "URCV" Receive asynchronous data from a remote partner SFB with the type "USEND"
SFB 12 SFB 13	BSEND BRCV	Send data to a remote partner SFB with the type "BRCV" Receive asynchronous data from a remote partner SFB with the type "BSEND" With this data transfer, a larger amount of data can be transported between the communication partners than is possible with all other communications SFBs for the configured S7 connections.
SFB 14	GET	Read data from a remote CPU
SFB 15	PUT	Write data to a remote CPU
SFB 16	PRINT	Send data to printer
SFB 19	START	Carry out a warm restart or cold start in a remote station
SFB 20	STOP	Set a remote station to STOP state
SFB 21	RESUME	Carry out a restart in a remote station
SFB 22	STATUS	Query the device status of a remote partner
SFB 23	USTATUS	Uncoordinated receiving of a remote device status

Integration in STEP7

S7 communication offers communication functions through configured S7 connections. You use STEP 7 to configure the connections.

S7 connections with an S7-400 are established when loading the connection data.

4.2.6 Global data communication

Properties

Global data communication is used for cyclic exchange of global data via MPI subnets (for example, I, Q, M) between SIMATIC S7 CPUs. The data communication is unacknowledged. One CPU broadcasts its data to all other CPUs on the MPI subnet.

The integrated communication functions are called via SFCs in the user program.

SFCs for the Global Data Communication

The following SFCs are integrated in the operating system of the S7-400 CPUs:

Table 4-4 SFCs for the Global Data Communication

Block	Block name	Brief description
SFC 60	GD_SEND	Collect and send data of a GD packet
SFC 61	GD_REC	Fetch data of an arrived GD message frame and enter it in the receive GD packet.

Reduction ratio

The reduction ratio specifies the cyclic intervals for GD communication. You set the reduction ratio when you configure global data communication in STEP 7. For example, if you set a reduction ratio of 7, global data communication is performed every 7th cycle. This reduces the load on the CPU.

Send and Receive Conditions

Meet the following conditions for communication via GD circuits:

- For the transmitter of a GD packet:
  $\text{Reduction ratio}_{\text{transmitter}} \times \text{cycle time}_{\text{transmitter}} \geq 60\ \text{ms}$
- For the receiver of a GD packet:
  $\text{Reduction ratio}_{\text{receiver}} \times \text{cycle time}_{\text{receiver}} < \text{reduction ratio}_{\text{transmitter}} \times \text{cycle time}_{\text{transmitter}}$

A GD packet may be lost if you do not adhere to these conditions. The reasons being:

- The performance of the "smallest" CPU in the GD circuit
- Transmission and reception of global data is performed asynchronously at the stations.

When setting in STEP 7: “Transmit after each CPU cycle“, and the CPU has a scan cycle time < 60 ms, the operating system might overwrite a GD packet of the CPU before it is transmitted. The loss of global data is indicated in the status box of a GD circuit, if you set this function in your STEP 7 configuration.

GD resources of the CPUs

Table 4-5 GD resources of the CPUs

Parameters	CPU 414-3 PN/DP	CPU 416-3 PN/DP
Number of GD circuits per CPU	Max. 8	Max. 16
GD packets transmitted by all GD circuits	Max. 8	Max. 16
GD packets received by all GD circuits	Max. 16	Max. 32
Data length per GD packet	Max. 54 bytes	Max. 54 bytes
Consistency	1 variable	1 variable

4.2.7 Routing

Properties

You can access other stations on other subnets with the programming device / PC of your S7 stations. You can use this for the following actions:

- Downloading user programs
- Downloading a hardware configuration
- Performing testing and diagnostics functions

Note

If you use your CPU as I-slave, the routing function is only possible when the DP interface is switched to active In STEP 7, set the Test, Commission Routing check box in the properties dialog of the DP interface. For detailed information, refer to the *Programming with STEP 7* manual, or directly to the *STEP 7 Online Help*

Requirements

- The station modules are "capable of routing" (CPUs or CPs).
- The network configuration does not exceed project limits.
- The modules have loaded the configuration data containing the latest "knowledge" of the entire network configuration of the project.

  Reason: All modules participating in the network transition must receive the routing information defining the paths to other subnets.
- In your network configuration, the PG/PC you want to use to establish a connection via network node must be assigned to the network it is physically connected to.
- The CPU must set to master mode, or
- when set to operate in slave mode, the Test, Commissioning, Routing functionality must be enabled by setting the check box in STEP 7, in the DP interface for DP slave properties dialog box.

Routing gateways: MPI - DP

Gateways between subnets are routed in a SIMATIC station that is equipped with interfaces to the respective subnets. The following figure shows CPU 1 (DP master) acting as router for subnets 1 and 2.

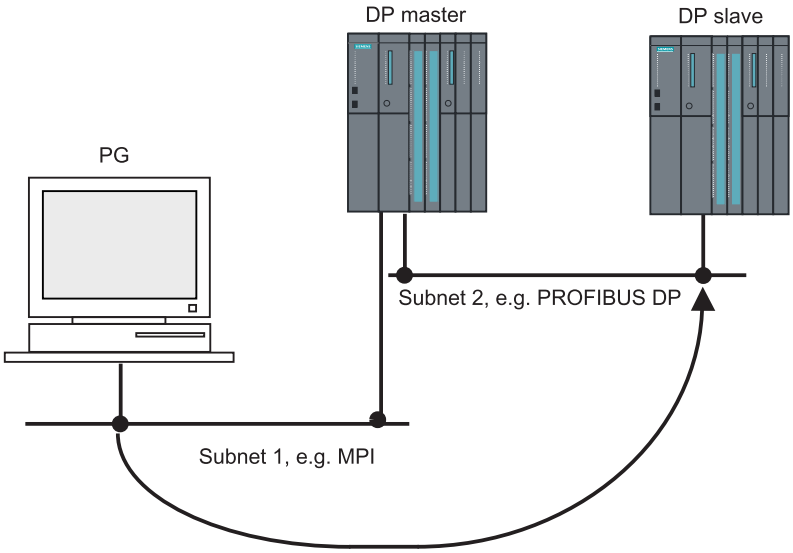


Figure 4-1 Routing

Routing Gateways: MPI - DP - PROFINET

The following figure shows access from MPI to PROFINET via PROFIBUS. CPU 1, for example 416-3, is the router for subnet 1 and 2; CPU 2 is the router for subnet 2 and 3.

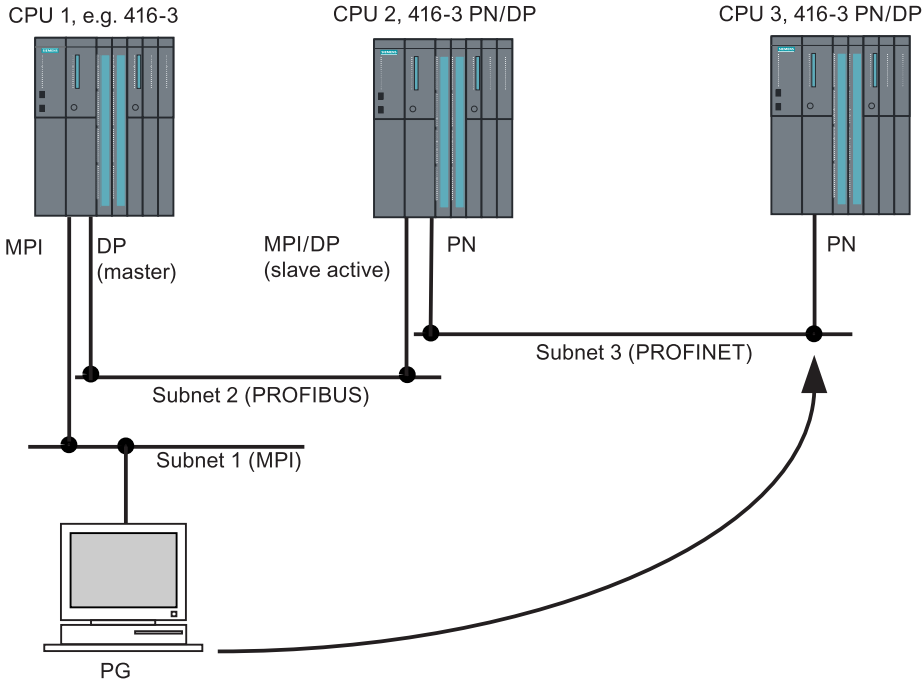


Figure 4-2 Routing gateways: MPI - DP - PROFINET

Routing: Example of a TeleService application

The following figure shows the example of an application for remote maintenance of an S7 station using a PG. The connection to other subnets is here established via modem connection.

The lower section of the figure shows how this can be configured in STEP 7.

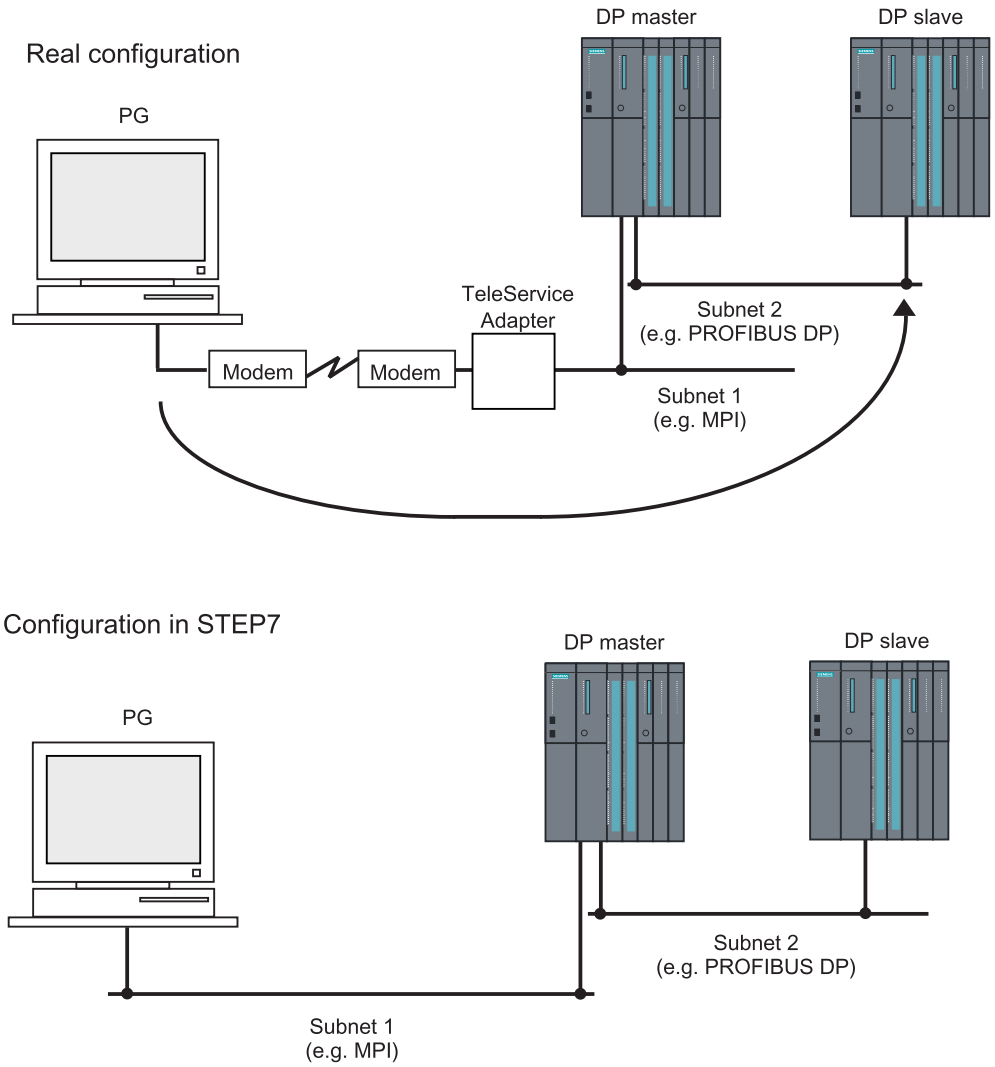


Figure 4-3 Routing: Example of a TeleService application

Reference

- You can find additional information on configuration with STEP 7 in the *Configuring Hardware and Connections with STEP 7* manual
- You can find more basic information in the *Communication with SIMATIC* manual.
- You can find additional information about the TeleService adapter under article ID 20983182 on the Internet at http://support.automation.siemens.com.
- You can find additional information on SFCs in the *Instruction List*.
  You can find a detailed description in the *STEP 7 Online Help* or *System and Standard Functions* reference manual.

4.3 S7 connections

4.3.1 Communication path of an S7 connection

An S7 connection is established as a communication channel when S7 modules communicate with one another.

Note

Global data communication, point-to-point connection via CP 341, PROFIBUS DP, PROFINET CBA, PROFINET IO, Web and SNMP require no S7 connections.

Every communication link requires S7 connection resources on the CPU for the entire duration of this connection.

Thus, every S7 CPU provides a specific number of S7 connection resources. These are used by various communication services (PG/OP communication, S7 communication or S7 basic communication).

Connection points

An S7 connection between modules with communication capability is established between connection points. The S7 connection always has two connection points, one active and one passive:

- The active connection point is assigned to the module that establishes the S7 connection.
- The passive connection point is assigned to the module that accepts the S7 connection.

Any module that is capable of communication can thus act as an S7 connection point. At the connection point, the established communication link always uses one S7 connection of the module concerned.

Transition point

If you use the routing functionality, the S7 connection between two modules capable of communication is established across a number of subnets. These subnets are interconnected via a network transition. The module that implements this network transition is known as a router. The router is thus the point through which an S7 connection passes.

Any CPU with a DP or PN interface can be the router for an S7 connection. The number of S7 connections limits the number of routing connections.

4.3.2 Assignment of S7 connections

There are several ways to allocate S7 connections on a communication-capable module:

- Reservation during configuration
- Assigning connections in the program
- Allocating connections during commissioning, testing and diagnostics routines
- Allocating connection resources to OCMS services

Reservation during configuration

One connection resource each is automatically reserved on the CPU for PG and OP communication. Whenever you need more connection resources, for example, when connecting several OPs, increase the number in the CPU properties dialog box in STEP 7.

Connections must also be configured (using NetPro) for the use of S7 communication. For this purpose, connection resources have to be available, which are not allocated to PG/OP or other connections. The required S7 connections are then permanently allocated for S7 communication when the configuration is uploaded to the CPU.

Assigning connections in the program

In basic S7 communication and in open Industrial Ethernet communication with TCP/IP, the user program establishes the connections. The CPU operating system initiates the connection. S7 basic communication uses the corresponding S7 connections. The open IE communication does not use any S7 connections.

Using connections for commissioning, testing and diagnostics

An active online function on the engineering station (PG/PC with STEP 7) occupies S7 connections for PG communication:

- If an S7 connection resource for PG communication is reserved in your CPU hardware configuration, it is assigned to the engineering station, that is, it only needs to be allocated.
- If all reserved S7 connection resources for PG communication are allocated, the operating system automatically assigns an available connection. If no more connection resources are available, the engineering station cannot communicate online with the CPU.

Allocating connection resources to OCMS services

S7 connection resources are allocated for the OP communication by an online function on the HMI station (OP/TP/... with *WinCC*) according to the following rules:

- If an S7 connection resource for OP communication is reserved in your CPU hardware configuration, it is assigned to this HMI station, that is, it only needs to be allocated.
- If all reserved S7 connection resources for OP communication are allocated, the operating system automatically assigns an available connection. If no more connection resources are available, the HMI station cannot communicate online with the CPU.

Time sequence for allocation of S7 connection resources

When you configure your project in STEP 7, the system generates parameter assignment blocks which are read by the modules during startup. This allows the module's operating system to reserve or allocate the relevant S7 connection resources. That is, for instance, OPs cannot access a reserved S7 connection resource for PG communication. The CPU's S7 connection resources which were not reserved can be used freely. These S7 connection resources are allocated in the order they are requested.

Example:

If there is only one free S7 connection left on the CPU, you can still connect a PG to the bus. The PG can then communicate with the CPU. The S7 connection is only used, however, when the PG is communicating with the CPU. If you connect an OP to the bus while the PG is not communicating, the OP can establish a connection to the CPU. Since an OP maintains its communication link at all times, in contrast to the PG, you cannot subsequently establish another connection via the PG.

4.3.3 Distribution and availability of S7 connection resources

Distribution of connection resources

Table 4-6 Distribution of connections

Communication service	Distribution
Programming device communication OP communication S7 basic communication	In order to avoid allocation of connection resources being dependent only on the chronological sequence in which various communication services are requested, connection resources can be reserved for these services. For PG and OP communication respectively, at least one connection resource is reserved by default. In the table below, and in the technical data of the CPUs, you can find the configurable S7 connection resources and the default configuration for each CPU. You "redistribute“ connection resources by setting the relevant CPU parameters in STEP 7.
S7 communication Other communication connections (e. g. via CP)	Available connection resources that are not specially reserved for a service (PG/OP communication, S7 basis communication) are used for this.
Routing PG functions	
Global data communication Point-to-point communication	This communication service uses no S7 connection resources.
PROFIBUS DP	This communication service uses no S7 connection resources.
PROFINET CBA	This communication service uses no S7 connection resources.
PROFINET IO	This communication service uses no S7 connection resources.
Open communication by means of TCP/IP	This communication service uses S7 connection resources.
Open communication by means of ISO on TCP	This communication service uses S7 connection resources.
Open communication by means of UDP	This communication service uses S7 connection resources.
Web	This communication service uses no S7 connection resources.
SNMP	This communication service uses no S7 connection resources.

Availability of connection resources

Table 4-7 Availability of connection resources

CPU	Total number connection resources	Reserved for		Free S7 connections
		Programming device communication	OP communication	
416-3 PN/DP	64	1	1	Displays all non-reserved S7 connection resources as free connection resources.
414-3 PN/DP	32	1	1	

PROFIBUS DP

5

5.1 CPU 41x-3 PN/DP as DP master / DP slave

5.1.1 Overview

Introduction

This chapter describes the properties and technical specifications that you require when you use a CPU 41x-3 PN/DP as a DP master or as a DP slave and configure it for direct data exchange.

Declaration: Since the DP master / DP slave response is the same for all CPUs, we will therefore simply refer to the CPUs in the following as CPU 41x-3 PN/DP.

Further Information

For information on the hardware and software configuration of a PROFIBUS subnet and on diagnostic functions within the PROFIBUS subnet, refer to the STEP 7 Online Help.

5.1.2 DP address areas of 41x CPUs

Address Areas of 41x CPUs

Table 5-1 41x CPUs (MPI/DP interface and DP module as PROFIBUS DP)

Address area	414-3	416-3
MPI interface as PROFIBUS DP, both inputs and outputs (bytes)	2048	2048
DP interface as PROFIBUS DP, both inputs and outputs (bytes)	6144	8192
DP module as PROFIBUS DP, both inputs and outputs (bytes)	6144	8192
In the process image, both inputs and outputs	8192	16384

In the input address area, the DP diagnostic addresses occupy at least 1 byte for the DP master and each DP slave. The DP standard diagnostics for each node can be called at these addresses, for example (LADDR parameter of SFC13). You specify the DP diagnostic addresses during project engineering. If you do not specify DP diagnostic addresses, STEP 7 assigns the addresses as DP diagnostic addresses in descending order starting at the highest byte address.

In the DPV1 master mode, the slaves are usually assigned two diagnostic addresses.

5.1.3 CPU 41x as PROFIBUS DP master

Introduction

This section describes the properties and technical specifications of the CPU if you operate it as a PROFIBUS DP master.

Reference

You can find the features and technical specifications of the 41x CPUs as of in this manual in *Technical specifications*.

Requirement

You need to configure the relevant CPU interface for operation in DP master mode. This means that you do the following in *STEP 7*:

1. Configure the CPU as a DP master
2. Assign a PROFIBUS address.
3. Select an operating mode (S7-compatible or DPV1).
4. Assign a diagnostic address.
5. Connect DP slaves to the DP master system.

Note

Is one of the PROFIBUS DP slaves a CPU 31x or CPU 41x?

If yes, you will find it in the PROFIBUS DP catalog as a "preconfigured station". Assign this DP slave CPU a slave diagnostic address in the DP master. Interconnect the DP master with the DP slave, and define the address areas for data exchange with the DP slave CPU.

From EN 50170 to DPV1

Enhancement of the distributed I/O EN 50170 standard. The results were incorporated into IEC 61158 / IEC 61784-1:2002 Ed1 CP 3/1. The SIMATIC documentation refers to this as DPV1.

Modes for DPV1 components

- S7-compatible mode

  In this mode, the components are compatible with EN 50170. Note that you cannot utilize the full DPV1 functionality in this mode.

- DPV1 mode

  In this mode, you can utilize the full DPV1 functionality. Automation components in the station that do not support DPV1 can be used as before.

DPV1 and EN 50170 compatibility

You can continue to use all existing slaves after the system conversion to DPV1. These do not, however, support the enhanced function of DPV1.

DPV1 slaves can be used in systems that are not converted to DPV1. In this case, their behavior corresponds with that of conventional slaves. SIEMENS DPV1 slaves can be operated in S7-compatible mode. For the DPV1 slaves of other manufacturers, you need a GSD file < Rev. 3 file to EN 50170.

Further Information

Information on the migration from EN 50170 to DPV1 is available on the Internet, on the FAQ pages "Changing from EN 50170 to DPV1", FAQ ID 7027576, of the Customer Support.

`http://www.siemens.com/automation/service&support`

Monitor/Modify, Programming via PROFIBUS

As an alternative to the MPI interface, you can use the PROFIBUS DP interface to program the CPU or execute the programming device functions Monitor and Modify.

Note

The execution of programming and monitor/modify functions via PROFIBUS DP interface prolongs the DP cycle.

Constant bus cycle time

This is a property of PROFIBUS DP. The "Constant bus cycle time" function ensures that the DP master always starts the DP bus cycle within a constant interval. From the perspective of the slaves, this means that they receive their data from the master at constant time intervals.

In STEP 7 V 5.2 or higher, you can configure constant bus cycle times for PROFIBUS subnets.

Isochronous Updating of Process Image Partitions

SFC126 "SYNC_PI" is used for the isochronous update of the process image partition of inputs. An application program which is interconnected to a DP cycle can use the SFC for consistent updates of the data recorded in the process image partition of inputs in synchronism with this cycle. SFC126 accepts interrupt control and can only be called in the OBs 61, 62, 63 and 64.

SFC 127 "SYNC_PO" is used for the isochronous update of the process image partition of outputs. An application program which is interconnected to a DP cycle can use the SFC for the consistent transfer of the computed output data of a process image partition of outputs to the I/O in synchronism with this cycle. SFC127 accepts interrupt control and can only be called in the OBs 61, 62, 63 and 64.

To allow isochronous updates of process image partitions, all input or output addresses of a slave must be assigned to the same process image partition.

To ensure consistency of data in a process image partition, the following conditions must be satisfied on the various CPUs:

- CPU 414: Number of slaves + number of bytes / 100 < 26
- CPU 416: Number of slaves + number of bytes / 100 < 40

The SFCs 126 and 127 are described in the corresponding Online Help and in the "*System and Standard Functions*" manual.

Consistent User Data

Data that belongs together in terms of its content and describes a process state at a specific point in time is known as consistent data. To maintain consistency, the data should not be changed or updated during processing or transmission.

You will find a detailed description of this procedure in Subsection *Consistent User Data*.

Sync/Freeze

The SYNC control command is used to set sync mode on the DP slaves of selected groups. In other words, the DP master transfers current output data and instructs the relevant DP slaves to freeze their outputs. The DP slaves writes the output data of the next output frames to an internal buffer; the state of the outputs remains unchanged.

Following each SYNC control command, the DP slaves of the selected groups transfer the output data stored in the internal buffer to the process outputs.

The outputs are only updated cyclically again after you transfer the UNSYNC control command using SFC11 "DPSYC_FR".

The FREEZE control command is used to set the relevant DP slaves to Freeze mode, in other words, the DP master instructs the DP slaves to freeze the current state of the inputs. It then transfers the frozen data to the input area of the CPU.

Following each FREEZE control command, the DP slaves freeze the state of their inputs again.

The DP master receives the current state of the inputs cyclically again not until you have sent the UNFREEZE control command with SFC11 "DPSYC_FR".

For information on SFC11, refer to the corresponding online help and to the *System and Standard Functions* manual

Startup of the DP Master System

Use the following parameters to set startup monitoring of the DP master:

- Transfer of the parameters to modules
- "Ready" message from the module

That is, the DP slaves must start up within the set time and be configured by the CPU (as DP master).

PROFIBUS Address of the DP Master

All PROFIBUS addresses are allowed.

5.1.4 Diagnostics of the CPU 41x as DP master

Diagnostics using LEDs

The following table explains the meaning of the BUSF LED. The BUSF LED assigned to the interface configured as the PROFIBUS DP interface will always light up or flash.

Table 5-2 Meaning of the "BUSF" LED of the CPU 41x as DP master

BUSF	Meaning	Remedy
Off	Configuration correct; All configured slaves can be addressed	–
Lit	• Bus fault (hardware fault) • DP interface fault • Different transmission rates in multi-DP master mode	• Check for short-circuit or interruption of the bus cable. • Evaluate the diagnostics. Reconfigure or correct the configuration.
Flashing	• Station failure • At least one of the assigned slaves cannot be addressed	• Check whether the bus cable is connected to the CPU 41x or whether the bus is interrupted. • Wait until the CPU 41x has started up. If the LED does not stop flashing, check the DP slaves or analyze the diagnostic data of the DP slaves.
flashes briefly INTF lights up briefly	CiR synchronization running	–

Triggering Detection of the Bus Topology in a DP Master System with the SFC103 "DP_TOPOL"

The diagnostic repeater is available to improve the ability to locate faulty modules or an interruption on the DP cable when failures occur in ongoing operation. This module operates as a slave and can identify the topology of a DP chain and record any faults originating from it.

You can use SFC103 "DP_TOPOL" to trigger the identification of the bus topology of a DP master system by the diagnostic repeater. For information on SFC103, refer to the corresponding online help and to the *System and Standard Functions* manual. The diagnostic repeater is described in the manual *Diagnostic Repeater for PROFIBUS DP*, Order Number 6ES7972-0AB00-8BA0.

Reading Out Diagnostic Data with *STEP 7*

Table 5-3 Reading out the diagnostics with STEP 7

DP master	Block or tab in *STEP 7*	Application	Reference
CPU 41x	"DP Slave Diagnostics" tab	Show slave diagnosis in clear text on the *STEP 7* interface	See the section on hardware diagnostics in the *STEP 7* online help system and in the *Programming with STEP 7* manual
	SFC13 "DPNRM_DG"	Reading out slave diagnostics (store in data area of the user program)	SFC, see *System Software for S7-300/400, System and Standard Functions* reference manual. For the structure of other slaves, refer to their descriptions.
	SFC59 "RD_REC"	Reading the data records of S7 diagnostics (stored in the data area of the user program)	*System Software for S7-300/400, System and Standard Functions* reference manual.
	SFC 51 "RDSYSST"	To read out partial SSL lists. Call SFC51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	
	SFB 52 "RDREC"	For DPV1 slaves Reading the data records of S7 diagnostics (stored in the data area of the user program)	
	SFB 54 "RALRM"	For DPV1 slaves: To read out interrupt information within the associated interrupt OB	
	SFC 103 "DP_TOPOL"	Triggers detection of the bus topology of a DP master system with diagnostic repeaters installed there.	

Analysis of Diagnostic Data in the User Program

The following figure shows you how to evaluate the diagnostic data in the user program.

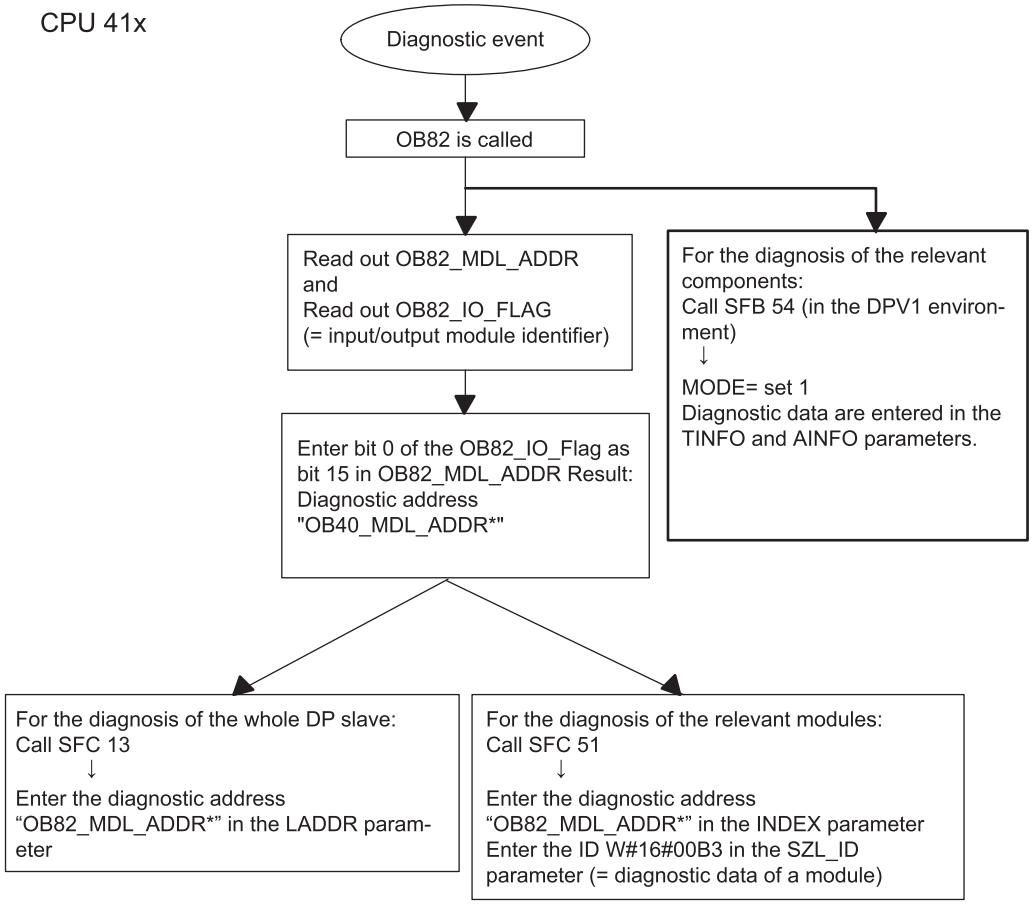
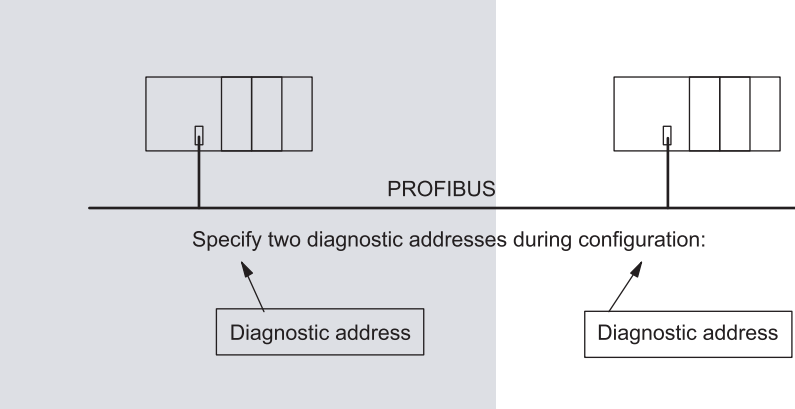


Figure 5-1 Diagnostics with CPU 41x

Diagnostic Addresses in Connection with DP Slave Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Verify in your configuration that the DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

Table 5-4 Diagnostic addresses for the DP master and DP slave

S7 CPU as DP master	S7 CPU as DP slave
	
During the configuration of the DP master, you specify (in the associated project of the DP master) a diagnostic address for the DP slave. Below, this diagnostic address is labeled *assigned to DP master*. By means of this diagnostic address the DP master receives information on the status of the DP slave or a bus interruption (see also table "Event detection of the CPUs 41x as DP master").	During the configuration of the DP slave, you also specify (in the associated project of the DP slave) a diagnostic address that is *assigned to the DP slave*. Below, this diagnostic address is labeled assigned to DP slave. By means of this diagnostic address the DP slave receives information on the status of the DP master or a bus interruption (see also table "Event detection of the CPUs 41x as DP slave").

Event Recognition

The following table shows you how the CPU 41x as DP master detects any changes in the operating mode of a CPU as DP slave or interruptions in data transfer.

Table 5-5 Event detection of the CPUs 41x as DP master

Event	What happens in the DP master
Bus interruption (short-circuit, connector removed)	• OB86 called with the message station failure (event entering state; diagnostic address of the DP slave that is assigned to the DP master) • With I/O access: call of OB 122 (I/O access error)
DP slave: RUN → STOP	• OB82 is called with the message faulty module (event entering state; diagnostic address of the DP slave that is assigned to the DP master; variable OB82_MDL_STOP=1)
DP slave: STOP → RUN	• OB82 is called with the message Module OK (event exiting state; diagnostic address of the DP slave that is assigned to the DP master; variable OB82_MDL_STOP=0)

Evaluation in the User Program

The following table shows you how, for example, you can evaluate RUN-STOP transitions of the DP slave in the DP master (see also table "Event detection of the CPUs 41x as DP master").

Table 5-6 Evaluation of RUN-STOP transitions of the DP slave in the DP master

In the DP master		In the DP slave (CPU 41x)
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**		Diagnostic addresses: (example) Slave diagnostic address=**422** **Master diagnostic address=not relevant**
The CPU calls OB82 with the following information, amongst other things: • OB82_MDL_ADDR:=**1022** • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:= module malfunction Tip: The CPU diagnostic buffer also contains this information You should also program the SFC "DPNRM_DG" in the user program to read out the DP slave diagnostic data. Use the SFB 54 in the DPV1 environment. It outputs the interrupt information in its entirety.	←	CPU: RUN → STOP CPU generates a DP slave diagnostic frame.

5.1.5 CPU 41x as DP slave

Introduction

This section describes the properties and technical specifications of the CPU if you operate it as a DP slave.

Reference

You can find the features and technical specifications of the 41x CPUs in the section *Technical Specifications*.

Requirements

- Only one DP interface of a CPU can be configured as a DP slave.
- Will the MPI/DP interface be a DP interface? If so, you must configure the interface as a DP interface.

  Before commissioning you must configure the CPU as a DP slave. In other words, you must do the following in STEP 7

  – Activate the CPU as a DP slave,

  – Assign a PROFIBUS address,

  – Assign a slave diagnostic address

  – Define the address areas for data transfer to the DP master

Configuration and Parameter Assignment Frame

When you configure and assign parameters to CPU 41x, you are supported by *STEP 7*. If you require a description of the configuration and parameter assignment frame to carry out a check with a bus monitor, for example, you will find it on the Internet at `http://www.ad.siemens.de/simatic-cs` under the entry ID 1452338.

Monitoring/Modifying and Programming via PROFIBUS

As an alternative to the MPI interface, you can use the PROFIBUS DP interface to program the CPU or execute the programming device functions Monitor and Modify. To do this, you must enable these functions when you configure the CPU as DP slave in *STEP 7*.

Note

The use of Programming or Monitor and Modify via the PROFIBUS DP interface extends the DP cycle.

Data Transfer Via an Transfer Memory

As a DP slave the CPU 41x makes an transfer memory available to PROFIBUS DP. Data transfer between the CPU as DP slave and the DP master always takes place via this transfer memory. Configure the following address areas: 244 bytes per input / output with a maximum of 32 bytes per module.

That is, the DP master writes its data to these transfer memory address areas, the CPU reads these data in the user program, and vice versa.

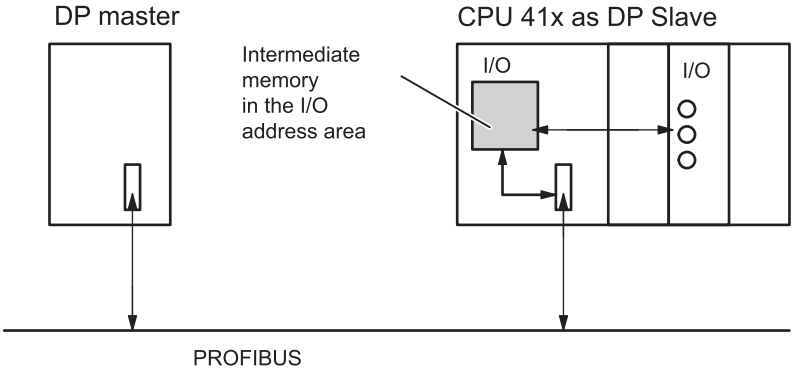


Figure 5-2 Transfer memory in the CPU 41x as DP slave

Address Areas of the Transfer Memory

Configure the input and output address areas in *STEP 7*:

- You can configure up to 32 input and output address areas.
- Each of these address areas can be up to 32 bytes in size.
- You can configure a maximum of 244 bytes of inputs and 244 bytes of outputs in total.

An example for the configuration of the address assignments of the transfer memory is provided in the table below. You will also find this in the online help for STEP 7 configuration.

Table 5-7 Configuration example for the address areas of the transfer memory

	Type	Master address	Type	Slave address	Length	Unit	Consistency
1	E	222	O	310	2	Byte	Unit
2	O	0	E	13	10	Word	Total length
:							
32							
	Address areas in the DP master CPU		Address areas in the DP slave CPU		These parameters of the address areas must be the same for the DP master and DP slave		

Rules

You must adhere to the following rules when working with the transfer memory:

- Assignment of the address areas:
  - Input data of the DP slave is **always** output data of the DP master
  - Output data of the DP slave is **always** input data of the DP master
- You can assign the addresses as you choose. You access the data in the user program with load/transfer commands or with SFCs 14 and 15. You can also specify addresses from the process image input and output table (see also section "DP address areas of the 41x CPUs").

Note

You assign addresses for the transfer memory from the DP address area of the CPU 41x.

You must not reassign the addresses you have already assigned to the transfer memory to the I/O modules on the CPU 41x.

- The lowest address in each address area is the start address of that address area.
- The length, unit and consistency of address areas for the DP master and DP slave that belong together must be the same.

S5 DP Master

If you use an IM 308 C as a DP master and the CPU 41x as a DP slave, the following applies to the exchange of consistent data:

You must program FB192 in the IM 308-C so that consistent data can be transferred between the DP master and DP slave. The data of the CPU 41x are only output or displayed contiguously in a block with FB192.

AG S5-95 as a DP Master

If you use an AG S5-95 as a DP master, you must also set its bus parameters for the CPU 41x as DP slave.

Sample Program

The small sample program below illustrates data transfer between the DP master and DP slave. This example contains the addresses from the table "Configuration example for the address areas of the transfer memory".

In the DP slave CPU

```
L        2                    Data
M        MB         6         preprocessing
L        IB         0         in the DP slave
M        MB         7
L        MW         6         Transfer data
M        PQW        310       to the DP
                              master

CALL     SFC        14        Receive data
 LADDR:=W#16#D                from the DP
 RET_VAL:=MW 20               master
 RECORD:=P#M30.0 Byte20
L        MB         30        Process
L        MB         7         received data
+        I
M        MW         100
```

In the DP master CPU

```
L        PIB        222       Process received
M        MB         50        data in the DP
L        PIB        223       master
L        B#16#3
+        I
M        MB         51

L        10                   Data
+        3                    preprocessing in
M        MB         60        the DP master

CALL     SFC        15        Send data to the
 LADDR:= W#16#0               DP slave
 RECORD:= P#M60.0 Byte20
 RET_VAL:= MW 22
```

Data Transfer in STOP Mode

The DP slave CPU changes to STOP mode: The data in the transfer memory of the CPU is overwritten with "0". In other words, the DP master reads "0".

The DP master changes to STOP mode: The current data in the transfer memory of the CPU is retained and can continue to be read by the CPU.

PROFIBUS Address

You must not set 126 as the PROFIBUS address for the CPU 41x as DP slave.

5.1.6 Diagnostics of the CPU 41x as DP slave

Diagnostics Using LEDs – CPU 41x

The following table explains the meaning of the BUSF LEDs. The BUSF LED assigned to the interface configured as the PROFIBUS DP interface is always lit or flashing.

Table 5-8 Meaning of the "BUSF" LEDs of the CPU 41x as DP slave

BUSF	Meaning	Remedy
Off	Configuration correct	–
Flashing	The parameter settings of the CPU 41x are incorrect. There is no data exchange between the DP master and the CPU 41x. Causes: • The response monitoring time has elapsed. • Bus communication over PROFIBUS DP has been interrupted. • The PROFIBUS address is incorrect.	• Check the CPU 41x. • Check to make sure that the bus connector is properly inserted. • Check whether the bus cable to the DP master has been disconnected. • Check the configuration and parameterization.
on	• Bus short-circuit	• Check the bus configuration

Detection of the Bus Topology in a DP Master System With the SFC103 "DP_TOPOL"

The diagnostic repeater is available to improve the ability to locate faulty modules or an interruption on the DP cable when failures occur in ongoing operation. This module operates as a slave and can identify the topology of a DP chain and record any faults originating from it.

You can use SFC103 "DP_TOPOL" to trigger the identification of the bus topology of a DP master system by the diagnostic repeater. For information on SFC103, refer to the corresponding online help and to the *System and Standard Functions* manual. The diagnostic repeater is described in the manual *Diagnostic Repeater for PROFIBUS DP*, Order Number 6ES7972-0AB00-8BA0.

Diagnostics with *STEP 5* or *STEP 7* Slave Diagnostics

The slave diagnostics complies with the EN 50170, Volume 2, PROFIBUS standard. Depending on the DP master, diagnostic information can be read out with *STEP 5* or *STEP 7* for all DP slaves that comply with the standard.

The display and structure of the slave diagnostics is described in the following sections.

S7 Diagnostics

S7 diagnostic information can be requested in the user program from all diagnostics-capable modules in the SIMATIC S7/M7 range of modules. You can find out which modules have diagnostic capability in the module information or in the catalog. The structure of the S7 diagnostic data is the same for both central and distributed modules.

The diagnostic data of a module is located in data records 0 and 1 of the system data area of the module. Data record 0 contains 4 bytes of diagnostic data describing the current status of a module. Data record 1 also contains module-specific diagnostic data.

You will find the structure of the diagnostic data described in the *Standard and System Functions* reference manual.

Reading Out the Diagnostics

Table 5-9 Reading out the diagnostic data with STEP 5 and STEP 7 in the master system

Automation system with DP master	Block or tab in *STEP 7*	Application	Reference
SIMATIC S7	"DP Slave Diagnostics" tab	Show slave diagnosis in clear text on the *STEP 7* interface	See the section on hardware diagnostics in the *STEP 7* online help system and in the *Programming with STEP 7* manual
	SFC13 "DP NRM_DG"	Reading out slave diagnostics (store in data area of the user program)	SFC, see *System Software for S7-300/400, System and Standard Functions* reference manual.
	SFC 51 "RDSYSST"	Read out partial SSL lists. Call SFC51 in the diagnostic interrupt using the SSL ID W#16#00B3 and read out the SSL of the slave CPU.	*System Software for S7-300/400, System and Standard Functions* reference manual.
	SFB54 "RDREC"	The following applies to the DPV1 environment: To read out interrupt information within the associated interrupt OB	
	FB125/FC125	To evaluate slave diagnostic information	The Internet page `http://www.ad.siemens.de/simatic-cs` ID 387 257
SIMATIC S5 with IM 308-C operating in DP master mode	FB 192 "IM308C"	Reading out slave diagnostics (store in data area of the user program)	For structure, see section "Diagnostics of the CPU 41x as DP slave"; FBs see manual *Distributed I/O Station ET 200*
SIMATIC S5 with the S5-95U programmable controller as DP master	FB 230 "S_DIAG"		

Example of Reading Slave Diagnostic Data, Using FB 192 "IM 308C"

Here, you will find an example of how to use FB 192 to read out the slave diagnostics for a DP slave in the STEP 5 user program.

Assumptions

For this STEP 5 user program, the following is assumed:

- The IM 308-C operating in DP master mode uses the page frames 0 to 15 (number 0 of IM 308-C).
- The DP slave is assigned PROFIBUS address 3.
- Slave diagnostics data should be stored in DB 20. You can also use any other data block for this.
- Slave diagnostic data has a length of 26 bytes.

STEP 5 User Program

Table 5-10 STEP 5 User Program

STL			Description
	:A	DB 30	Default address area for the IM 308-C
	:SPA	FB 192	IM no. = 0, PROFIBUS address of the DP slave = 3
Name	:IM308C		Function: Read slave diagnosis
DPAD	:	KH F800	is not evaluated
IMST	:	KY 0, 3	S5 data area: DB 20
FCT	:	KC SD	Diagnosis data as of data word 1
GCGR	:	KM 0	Length of diagnostic data = 26 bytes
TYPE		KY 0, 20	Error code storage in the DW 0 of the DB 30
STAD		KF +1	
LENG		KF 26	
ERR		DW 0	

Diagnostic Addresses in Connection with DP Master Functionality

You assign diagnostic addresses for the PROFIBUS DP in the CPU 41x. Verify in your configuration that the DP diagnostic addresses are assigned once to the DP master and once to the DP slave.

Table 5-11 Diagnostic addresses for the DP master and DP slave

S7 CPU as DP master	S7 CPU as DP slave
During the configuration of the DP master, you specify (in the associated project of the DP master) a diagnostic address for the DP slave. In the following, this diagnostic address is described as being assigned to the DP master. By means of this diagnostic address the DP master receives information on the status of the DP slave or a bus interruption (see also table "Event detection of the CPUs 41x as DP master").	During the configuration of the DP slave, you also specify (in the associated project of the DP slave) a diagnostic address that is assigned to the DP slave. Below, this diagnostic address is labeled assigned to DP slave. By means of this diagnostic address the DP slave receives information on the status of the DP master or a bus interruption (see also table "Event detection of the CPUs 41x as DP slave").

Event Detection

The following table shows you how the CPU 41x as DP slave detects any operating mode changes or interruptions in data transfer.

Table 5-12 Event detection of the CPUs 41x as DP slave

Event	What happens in the DP slave?
Bus interruption (short-circuit, connector removed)	• Calls OB86 with the message *Station failure* (incoming event; diagnostic address of the DP slave, assigned to the DP slave) • With I/O access: call of OB 122 (I/O access error)
DP master RUN → STOP	• Calls OB82 with the message *Module error* (incoming event; diagnostic address of the DP slave assigned to the DP slave; Variable OB82_MDL_STOP=1)
DP master STOP → RUN	• OB82 is called with the message *Module OK*(event exiting state; diagnostic address of the DP slave that is assigned to the DP slave; variable OB82_MDL_STOP=0)

Evaluation in the User Program

The table below shows an example of you how you can evaluate RUN-STOP transitions of the DP master in the DP slave (see also the previous table).

Table 5-13 Evaluating RUNSTOP transitions in the DP Master/DP Slave

In the DP master	In the DP slave (CPU 41x)
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**	Diagnostic addresses: (example) Slave diagnostic address=**422** **Master diagnostic address=not relevant**
CPU: RUN → STOP	The CPU calls OB82 with the following information, amongst other things: • OB82_MDL_ADDR:=422 • OB82_EV_CLASS:=B#16#39 (incoming event) • OB82_MDL_DEFECT:=module malfunction Tip: The CPU diagnostic buffer also contains this information

Structure of Slave Diagnostics

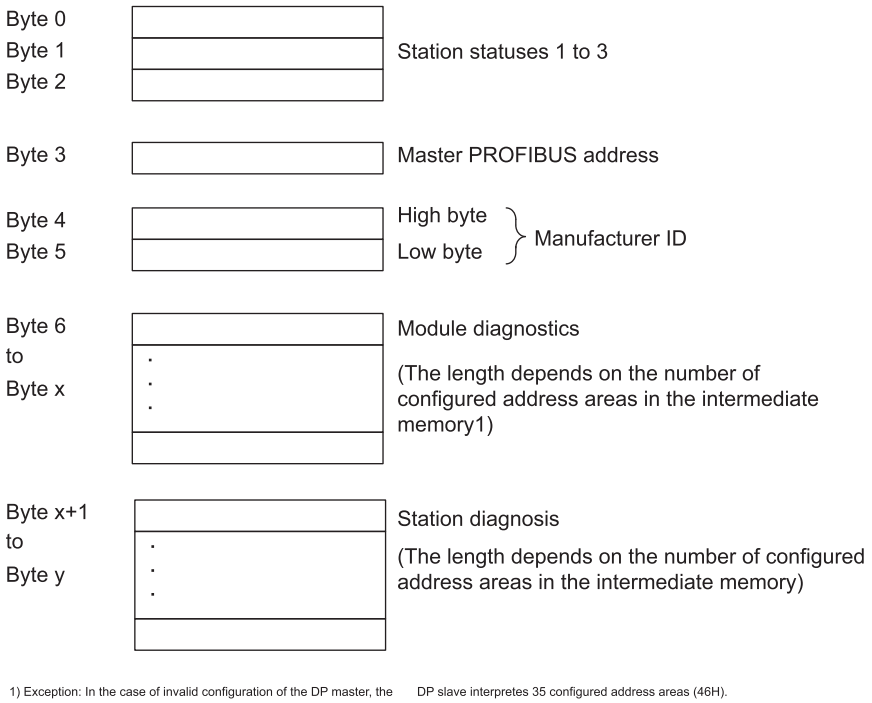


Figure 5-3 Structure of slave diagnostics

5.1.7 CPU 41x as DP slave: Station statuses 1 to 3

Station statuses 1 to 3

Station status 1 to 3 provides an overview of the status of a DP slave.

Table 5-14 Structure of station status 1 (Byte 0)

Bit	Meaning	Remedy
0	1:The DP slave cannot be addressed by the DP master.	• Correct DP address set on the DP slave? • Bus connector connected? • Voltage at DP slave? • RS-485 repeater set correctly? • Execute reset on the DP slave
1	1:The DP slave is not yet ready for data exchange.	• Wait while the DP slave powers up.
2	1:The configuration data sent by the DP master to the DP slave does not match the configuration of the DP slave.	• Correct station type or correct configuration of the DP slave entered in the software?
3	1:Diagnostic interrupt, triggered by RUN-STOP change on the CPU 0:Diagnostic interrupt, triggered by STOP-RUN change on the CPU	• You can read out the diagnostic information.
4	1:Function is not supported, e.g. changing the DP address via software	• Check the configuration.
5	0:The bit is always "0".	–
6	1:The DP slave type does not correspond to the software configuration.	• Correct station type entered in the software? (Parameter assignment error)
7	1:Parameters have been assigned to the DP slave by a different DP master to the one that currently has access to the DP slave.	• The bit is always 1, for example, if you access the DP slave with the programming device or another DP master. The DP address of the parameter assignment master is in the "master PROFIBUS address" diagnostic byte.

Table 5-15 Structure of station status 2 (Byte 1)

Bit	Meaning
0	1:The DP slave must be assigned new parameters and reconfigured.
1	1:There is a diagnostic message pending. The DP slave cannot continue until the problem has been eliminated (static diagnostic message).
2	1:The bit is always set to "1" if the DP slave with this DP address is present.
3	1:Watchdog monitoring is enabled for this DP slave.
4	0:The bit is always set to "0".
5	0:The bit is always set to "0".

Bit	Meaning
6	0:The bit is always set to "0".
7	1:The DP slave is disabled; in other words, it has been removed from cyclic processing.

Table 5-16 Structure of station status 3 (Byte 2)

Bit		Meaning
0 to 6	0:The bits are always set to "0".	
7	1:	• There are more diagnostic messages than the DP slave can store. • The DP master cannot enter all the diagnostic messages sent by the DP slave in its diagnostic buffer.

Master PROFIBUS Address

The master PROFIBUS address diagnostic byte contains the DP address of the DP master that:

- Assigned parameters to the DP slave and
- has read and write access to the DP slave

Table 5-17 Structure of the master PROFIBUS address (byte 3)

Bit	Meaning
0 to 7	DP address of the DP master that configured the DP slave and that has read and write access to the DP slave.
	FF_H: DP slave has not been assigned parameters by any DP master.

Identifier-related diagnostics

The ID-related diagnostic data tells you for which of the configured address areas of the transfer memory an entry has been made.

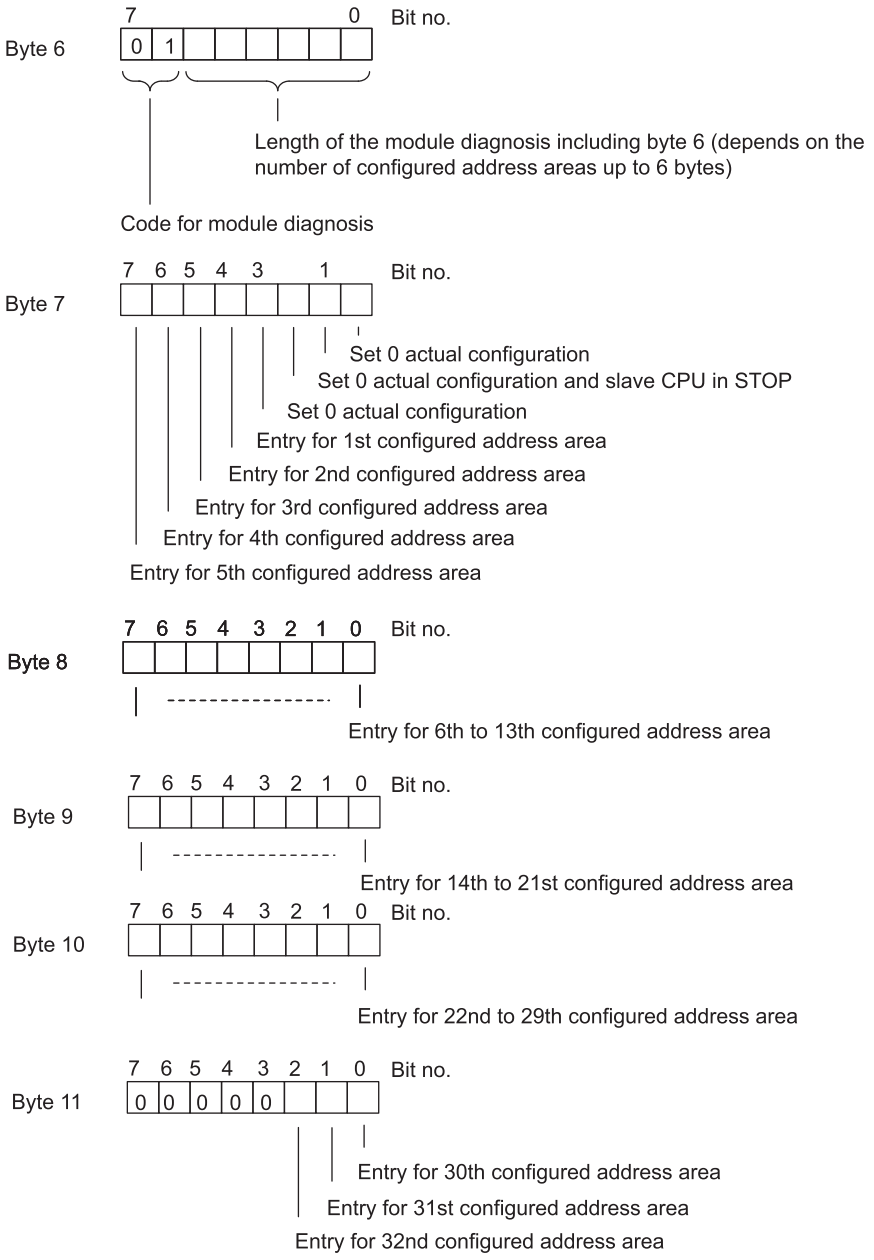


Figure 5-4 Structure of the ID-related diagnostic data of the CPU 41x

Device-Related Diagnostics

Device-related diagnostics provides detailed information on a DP slave. Device-related diagnostics starts at byte x and can include up to 20 bytes.

The figure below illustrates the structure and contents of the bytes for a configured address area of the transfer memory.

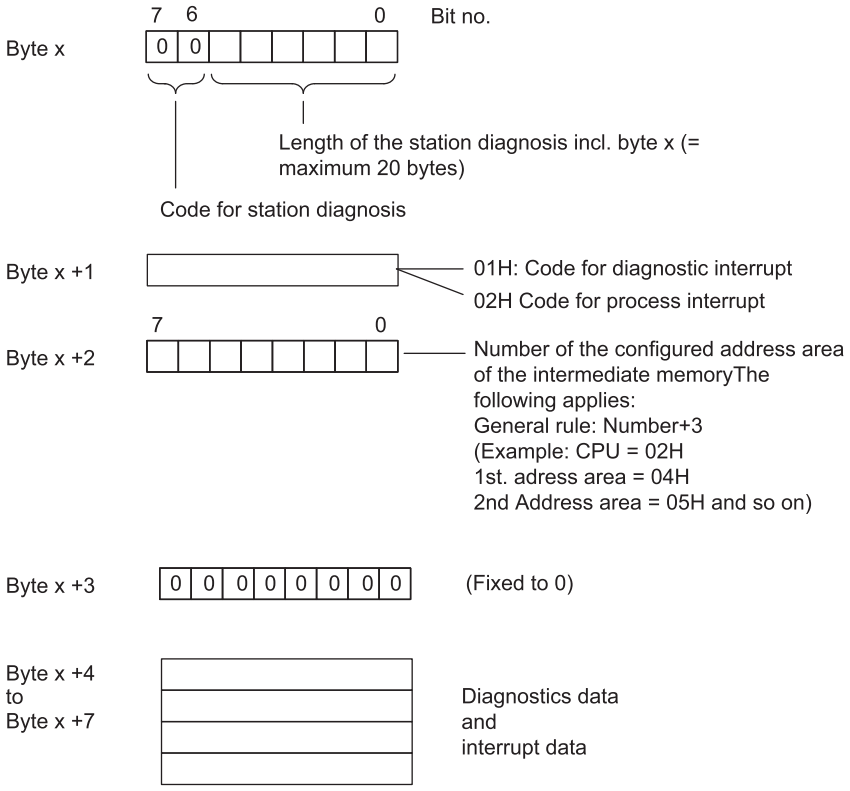


Figure 5-5 Structure of the device-related diagnostics

Starting at byte x +4

The meaning of the bytes starting at byte x+4 depends on byte x +1 (see figure "Structure of device-related diagnostics").

In byte x +1, the code stands for...	
Diagnostic interrupt (01_H)	**Hardware interrupt (02_H)**
The diagnostic data contains the 16 bytes of status information of the CPU. The figure below shows the allocation of the first four bytes of diagnostic data. The following 12 bytes are always 0.	You can program 4 bytes of interrupt information any way you wish for the process interrupt. You transfer these 4 bytes to the DP master in *STEP 7* using SFC7 "DP_PRAL".

Bytes x +4 to x +7 for Diagnostic Interrupts

The following figure illustrates the structure and contents of bytes x +4 to x +7 for the diagnostic interrupt. The data in these bytes correspond to the contents of data record 0 of diagnostic data in STEP 7 (in this case, not all bits are used).

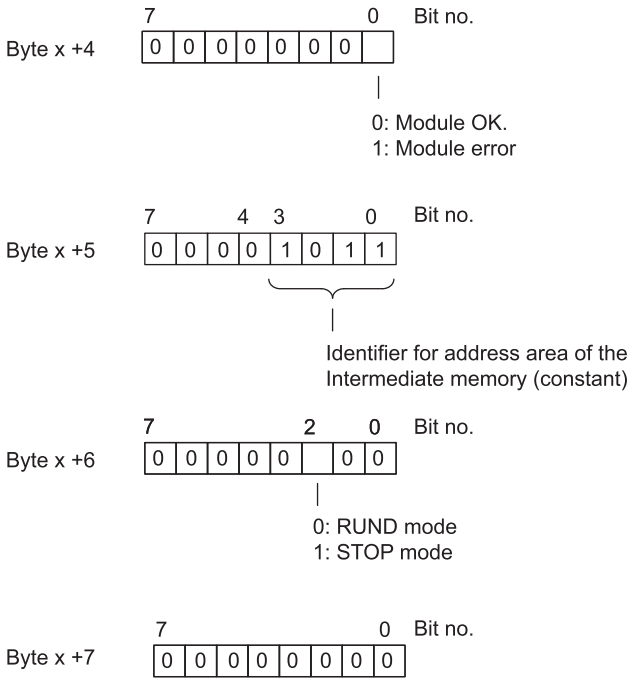


Figure 5-6 Bytes x +4 to x +7 for diagnostic and hardware interrupts

Interrupts with the S7 DP Master

In the CPU 41x as a DP slave you can trigger a process interrupt in the DP master from the user program. You can trigger an OB40 in the user program of the DP master by calling SFC7 "DP_PRAL". Using SFC7, you can forward interrupt information in a double word to the DP master and evaluate it in OB40 in the OB40_POINT_ADDR variable. You can program the interrupt information to suit your purposes. You will find a detailed description of SFC7 "DP_PRAL" in the *System Software for S7-300/400, System and Standard Functions* reference manual.

Interrupts with a Different DP Master

If you are operating the CPU 41x with a different DP master, these interrupts are simulated in the device-related diagnostic data of the CPU 41x. You have to process the relevant diagnostic events in the DP master's user program.

Note

Note the following in order to be able to evaluate diagnostic interrupts and hardware interrupts using device-related diagnostics when using a different DP master:

- the DP master should be able to save the diagnosis messages, i.e. the diagnosis messages should be stored within the DP master in a ring buffer. If there are more diagnostic messages than the DP master can store, then, for example, only the last diagnostic message received would be available for evaluation.
- You must scan the relevant bits in the device-related diagnostic data in your user program at regular intervals. You must also take the PROFIBUS DP bus cycle time into consideration so that, for example, you can query the bits at least once synchronized with the bus cycle time.
- With an IM 308-C operating in DP master mode, you cannot utilize process interrupts in device-specific diagnostics, because only incoming events are reported, rather than outgoing events.

5.1.8 Direct Data Exchange

5.1.8.1 Principle of direct data exchange

Overview

Direct data exchange is characterized by PROFIBUS DP nodes which "listen" on the bus and know which data a DP slave returns to its DP master.

This mechanism allows the "listening node" (recipient) direct access to deltas of input data of remote DP slaves.

In your STEP 7 configuration, define the address area of the recipient in which the required data of the publisher will be read, based on the peripheral input addresses.

A CPU 41x can be:

- DP slave sending station
- as DP slave or DP master or as CPU that is not linked into a master system (see Fig. 3-9).

Example:

The following figure uses an example to explain which direct data exchange "relations" you can configure. All the DP masters and DP slaves in the figure are 41x CPUs. Note that other DP slaves (ET 200M, ET 200X, ET 200S) can only be senders.

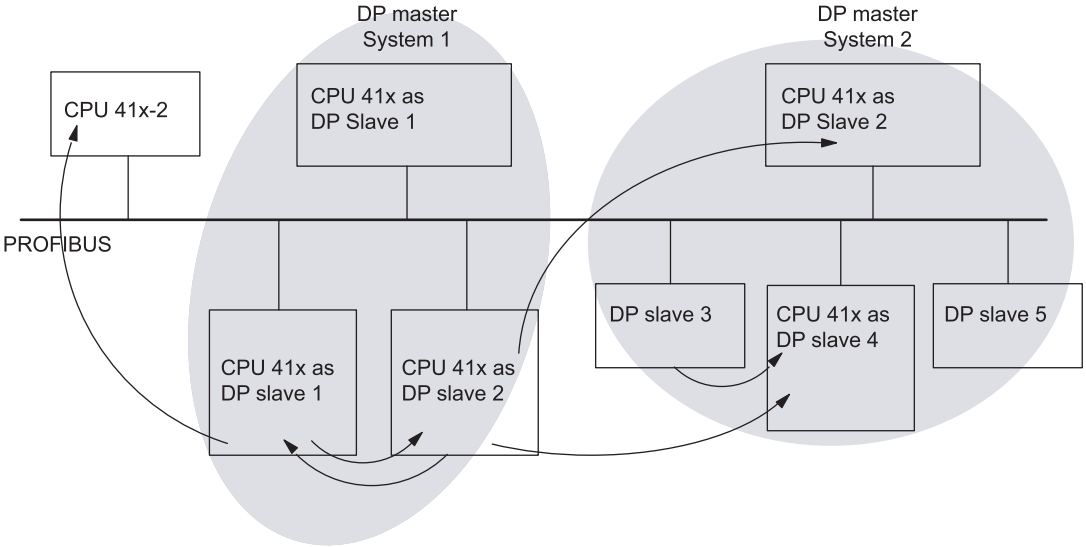


Figure 5-7 Direct data exchange with 41x CPUs

5.1.8.2 Diagnostics in direct data exchange

Diagnostic addresses

In direct data exchange you assign a diagnostic address in the recipient:

Table 5-18 Diagnostic address for the recipient during direct data exchange

S7-CPU as sender	S7-CPU as recipient
	
	During configuration you specify a diagnostic address in the recipient that is assigned to the sender. By means of this diagnostic address, the recipient obtains information on the status of the sender or a bus interruption (see also following table).

Event detection

The following table shows you how the CPU 41x as recipient detects interruptions in data transfer.

Table 5-19 Event detection of the 41x CPUs as recipients during direct communication

Event	What happens in the recipient
Bus interruption (short-circuit, connector removed)	• OB86 is called with the station failure message (event entering state; diagnostic address of the recipient assigned to the sender) • In the case of I/O access: OB122 called (I/O access error)

Evaluation in the user program

The following table shows you, for example, how you can evaluate a sender station failure in the recipient (see also table above).

Table 5-20 Evaluation of the station failure in the sender during direct data exchange

In the sender		In the recipient
Diagnostic addresses: (example) Master diagnostic address=**1023** Slave diagnostic address in the master system=**1022**		Diagnostic address: (example) Diagnostic address=**444**
Station failure	→	The CPU calls OB86 with the following information, amongst other things: • OB86_MDL_ADDR:=**444** • OB86_EV_CLASS:=B#16#38 (event entering state) • OB86_FLT_ID:=B#16#C4 (failure of a DP station) Tip: This information is also in the diagnostic buffer of the CPU

PROFINET

6

6.1 Introduction

What is PROFINET?

PROFINET is the open, non-proprietary Industrial Ethernet standard for automation. It enables comprehensive communication from the business management level down to the field level.

- PROFINET fulfills the high demands of industry, for example;
- Industrial-based installation engineering
- Real-time capability
- Isochronous motion control applications
- Non-proprietary engineering

A wide range of products from active and passive network components, controllers, distributed field devices to components for industrial wireless LAN and industrial security are available for PROFINET.

Documentation from PROFIBUS International on the Internet

Numerous texts on the subject of PROFINET are available from the URL "http://www.profinet.com" from PROFIBUS International (formerly PROFIBUS Nutzer-Organisation, PNO)

For further information, refer to Internet address "http://www.siemens.com\profinet\".

6.2 PROFINET IO and PROFINET CBA

PROFINET variations

There are two varieties of PROFINET

- PROFINET IO: IO devices are connected to an S7-400 CPU (IO controller) via Ethernet.
- PROFINET CBA: A component-based automation solution in which full technological modules are used as standardized components into large plants. You create the CBA components in SIMATIC with STEP 7 and the SIMATIC iMap add-on package. You connect the individual components with SIMATIC iMap.

  When you download CBA interconnections to an S7-400 CPU, they are stored in the working memory. The interconnections are lost if there is a defective hardware, a memory reset or firmware update.

  If you use Profinet CBA, you cannot use isochronous mode or perform configuration changes in runtime (CiR).

PROFINET IO and PROFINET CBA

PROFINET IO and PROFINET CBA are two different views of automation devices on Industrial Ethernet.

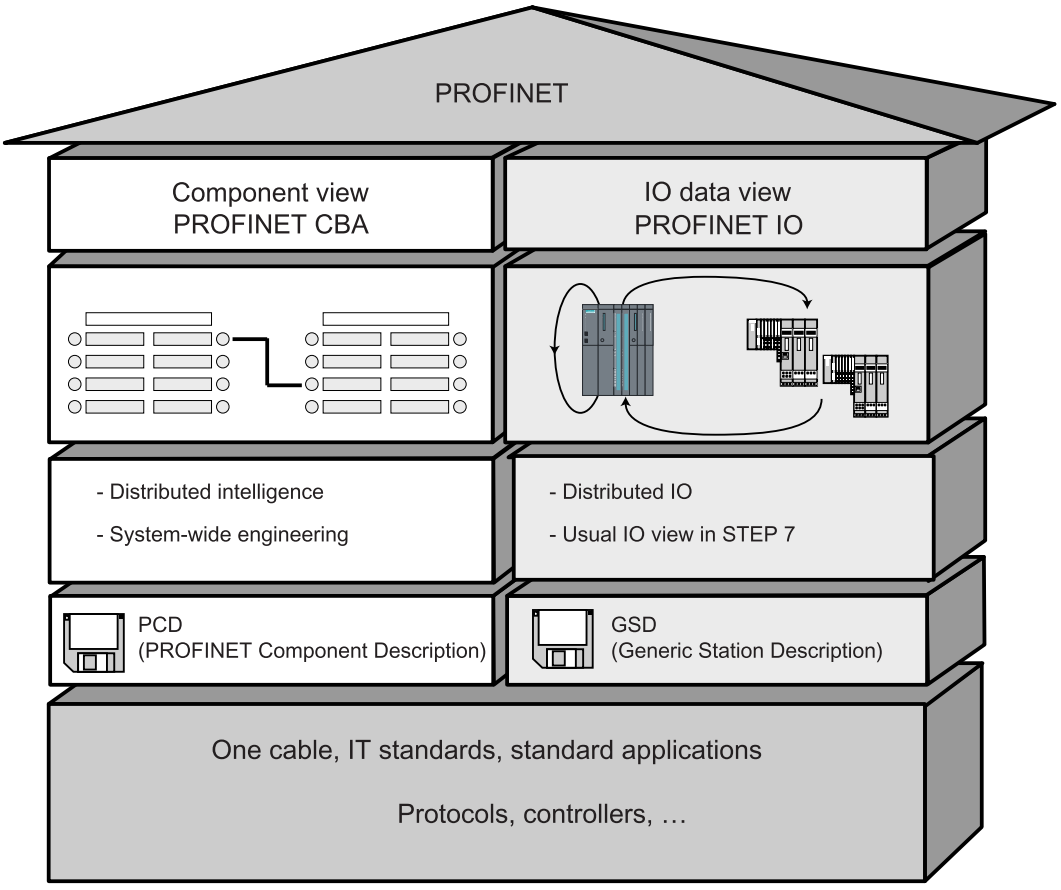


Figure 6-1 PROFINET IO and PROFINET CBA

PROFINET CBA divides an entire plant into various functions. These functions are configured and programmed.

PROFINET IO provides you with a view of the system that is very similar to the view obtained in PROFIBUS. You continue to configure and program the individual automation devices.

Reference

- Further information about PROFINET IO and PROFINET CBA is available in the *PROFINET System Description.*
- Differences between and common properties of the PROFIBUS DP and PROFINET IO are described in the *From PROFIBUS DP to PROFINET IO* Programming Manual.
- For further information about PROFINET CBA, refer to the documentation on SIMATIC iMAP and Component Based Automation.

6.3 PROFINET IO Systems

Extended Functions of PROFINET IO

The graphic below shows the new functions of PROFINET IO.

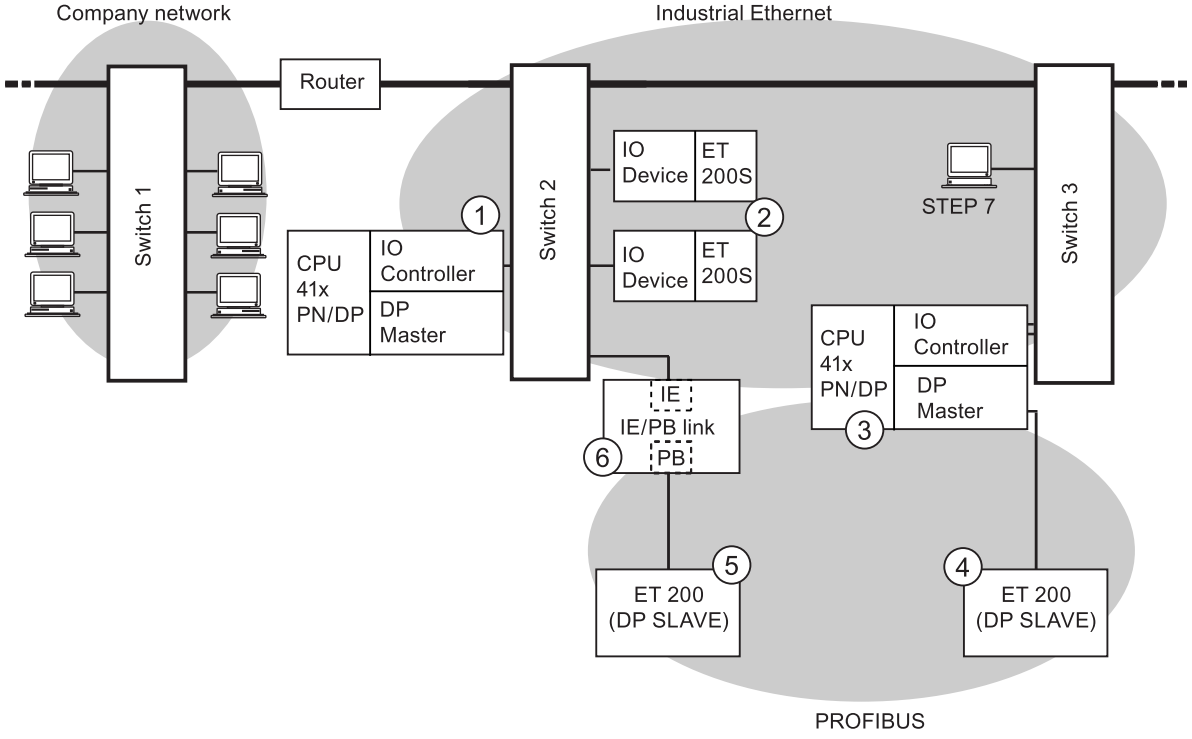


Figure 6-2 PROFINET IO

The figures show	Examples of connection paths
The connection of company network and field level	From PCs in your company network, you can access devices at the field level. Example: • PC - Switch 1 - Router - Switch 2 - CPU 41x PN/DP ①.
The connection between the automation system and field level	You can also access one of the other areas in Industrial Ethernet from an IO supervisor at the field level. Example: • IO-Supervisor - Switch 3 - Switch 2 - on an IO device of the ET 200S ②.
The IO controller of the CPU 41x PN/DP ① **directly** controls devices on the Industrial Ethernet and on the PROFIBUS	At this point, you see the extended IO feature between the IO controller and IO device(s) on Industrial Ethernet: • The CPU 41x PN/DP ①is the IO controller for one of the ET 200S ② IO-Devices. • The CPU 41x PN/DP ① is also the IO controller for the ET 200 (DP slave) ⑤ via the IE/PB Link ⑥.
A CPU can be both IO controller and DP master.	Here, you can see that a CPU can be both IO controller for an IO device as well as DP master for a DP slave: • The CPU 41x PN/DP ①is the IO controller for the other ET 200S ② IO-Devices. CPU 41x PN/DP ③ - Switch 3 - Switch 2 - ET 200S ② • The CPU 41x PN/DP ③ is the DP master for a DP slave ④. The DP slave ④ is assigned locally to the CPU ③ and is not visible on Industrial Ethernet.

Reference

For further information about PROFINET refer to the *From PROFIBUS DP to PROFINET IO programming manual.*
This manual also provides a comprehensive overview of the new PROFINET blocks and system status lists.

6.4 Blocks in PROFINET IO

Compatibility of the New Blocks

For PROFINET IO, some new blocks were created, among other things, because larger configurations are now possible with PROFINET. You can also use the new blocks with PROFIBUS.

Comparison of the System and Standard Functions of PROFINET IO and PROFIBUS DP

For CPUs with an integrated PROFINET interface, the table below provides you with an overview of the following functions:

- System and standard functions for SIMATIC that you may need to replace when converting from PROFIBUS DP to PROFINET IO.
- New system and standard functions

Table 6-1 New System and Standard Functions/System and Standard Functions to be Replaced

Blocks	PROFINET IO	PROFIBUS DP
SFC 12 Deactivation and activation of DP slaves/IO devices	Yes S7-400: As of firmware V5.0	Yes
SFC 13 Read diagnostic data of a DP slave	No Replacement: • Event-related: SFB 54 • State-related: SFB 52	Yes
SFC 58/59 Write/read record in the I(O devices.	No Replacement: SFB 53/52	Yes, if you have not already replaced these SFBs under DPV 1 by SFB 53/52.
SFB 53/52 Read/write record	Yes	Yes
SFB 54 Evaluate interrupts	Yes	Yes
SFB 81 Read predefined parameters	Yes	Yes
SFC 5 Query start address of a module	No Replacement: SFC 70	Yes
SFC 70 Query start address of a module	Yes	Yes
SFC 49 Query the slot belonging to a logical address	No Replacement: SFC 71	Yes

Blocks	PROFINET IO	PROFIBUS DP
SFC 71 Query the slot belonging to a logical address	Yes	Yes

The following table provides an overview of the system and standard functions for SIMATIC, whose functionality must be implemented by other functions when converting from PROFIBUS DP to PROFINET IO.

Table 6-2 System and Standard Functions in PROFIBUS DP that must be Implemented with Different Functions in PROFINET IO

Blocks	PROFINET IO	PROFIBUS DP
SFC 54 Read predefined parameters	No Replacement: SFB 81	Yes
SFC 55 Write dynamic parameters	No Replicate via SFB 53	Yes
SFC 56 Write predefined parameters	No Replicate via SFB 81 and SFB 53	Yes
SFC 57 Assigning module parameters	No Replicate via SFB 81 and SFB 53	Yes

You cannot use the following SIMATIC system and standard functions with PROFINET IO:

- SFC 7 Trigger hardware interrupt on DP master
- SFC 11 Synchronize groups of DP slaves
- SFC 72 Read data from a communication partner within local S7 station
- SFC 73 Write data to a communication partner within local S7 station
- SFC 74 Abort an existing connection to a communication partner within local S7 station
- SFC 103 Determine the bus typology in a DP master

Comparison of the Organization Blocks of PROFINET IO and PROFIBUS DP

The following table lists the changes at OBs 83 und OB 86:

Table 6-3 OBs in PROFINET IO and PROFIBUS DP

Blocks	PROFINET IO	PROFIBUS DP
OB 83 Removing and inserting modules during operation	New error information	Unchanged
OB 86 Rack failure	New error information	Unchanged

Detailed Information

For detailed descriptions of the individual blocks, refer to the manual *System Software for S7-300/400 System and Standard Functions*.

6.5 System status lists for PROFINET IO

Introduction

The CPU makes certain information available and stores this information in the "System status list".

The system status list describes the current status of the automation system. It provides an overview of the configuration, the current parameter assignment, the current statuses and sequences in the CPU, and the assigned modules.

The system status list data can only be read out, but not be changed. The system status list is a virtual list that is compiled only on request.

From a system status list you receive the following information via the PROFINET IO system:

- System data
- Module status information in the CPU
- Diagnostic data from a module
- Diagnostic buffer

Compatibility of the New System Status Lists

For PROFINET IO, some new system status lists were created, among other things, because larger configurations are now possible with PROFINET.

You can also use these new system status lists with PROFIBUS.

You can continue to use a known PROFIBUS system status list that is also supported by PROFINET. If you use a system status list in PROFINET that PROFINET does not support, an error code is returned in RET_VAL (8083: Index wrong or not permitted).

Comparison of the System Status Lists of PROFINET IO and PROFIBUS DP

Table 6-4 Comparison of the System Status Lists of PROFINET IO and PROFIBUS DP

SSL-ID	PROFINET IO	PROFIBUS DP	Applicability
W#16#0591	Yes Parameter adr1 changed	Yes	Module status information for the interfaces of a module
W#16#0C91	Yes Parameter adr1/adr2 and set/actual type identifier changed	Yes	Module status information of a module in a central configuration or attached to an integrated DP or PN interface, or an external DP interface using the logical address of the module.

SSL-ID	PROFINET IO	PROFIBUS DP	Applicability
W#16#4C91	Yes Parameter adr1 changed	Yes, internal interface No, external interface	Module status information of a module attached to an external DP or PN interface using the start address
W#16#0D91	Yes Parameter adr1 changed No, external interface	Yes, internal interface No, external interface	Module status information of all modules in the specified rack/station
W#16#0696	Yes, internal interface No, external interface	No	Module status information of all submodules on an internal interface of a module using the logical address of the module, not possible for submodule 0 (= module)
W#16#0C96	Yes	Yes, internal interface No, external interface	Module status information of a submodule using the logical address of this submodule
W#16#xy92	No Replacement: SSL-ID W#16#0x94	Yes	Rack/stations status information Replace this system status list with the system status list with ID W#16#xy94 in PROFIBUS DP, as well.
W#16#0x94	Yes	No	Rack/station status information

Detailed Information

For detailed descriptions of the individual system status lists, refer to the manual *System Software for S7-300/400 System and Standard Functions*.

6.6 Open Communication Via Industrial Ethernet

Requirement

- STEP 7 V5.4 + Servicepack 1 or higher

Functionality

CPUs with Firmware V5.0 or higher and integrated PROFINET interface support the open communication functionality via Industrial Ethernet (in short: *open IE communication*)

Following services are available for open IE communication:

- Connection oriented protocols:

  Prior to data transmission connection oriented protocols establish a logical connection to the communication partner and close this again, if necessary, after transmission is completed. Connection oriented protocols are used when security in especially important in data transmission. A physical cable can generally accommodate several logical connections. The maximum message frame length is 32 KB.

  The following connection oriented protocols are supported for the FBs for open IE communication:

  – TCP according to RFC 793

  – ISO on TCP according to RFC 1006

- Connectionless protocols:

  Connectionless protocols operate without a logical connection. There is also no establishing or terminating a connection to remote partner. Connectionless protocols transfer the data unacknowledged and thus unsecured to the remote partner. The maximum message frame length is 1472 bytes.
  The following connectionless protocols are supported for the FBs for open communication by means of Industrial Ethernet:

  – UDP according to RFC 768

How to use open IE communication

To allow data to be exchanged with other communication partners, STEP 7 provides the following FBs and UDTs under "Communication Blocks" in the "Standard Library":

- Connection oriented protocols: TCP/ISO-on-TCP
  – FB 63 "TSEND" for sending data
  – FB 64 "TRCV" for receiving data
  – FB 65 "TCON", for connecting
  – FB 66 "TDISCON", for disconnecting
  – UDT 65 "TCON_PAR" with the data structure for the configuration of the connection

- Connectionless protocol: UDP
  - FB 67 "TUSEND" for sending data
  - FB 68 "TURCV" for receiving data
  - FB 65 "TCON" for establishing the local communication access point
  - FB 66 "TDISCON" for resolving the local communication access point
  - UDT 65 "TCON_PAR" with the data structure for configuring the local communication access point
  - UDT 66 "TCON_ADR" with the data structure of the address parameters of the remote partner

Data blocks for the Configuration of the Connection

- Data blocks for configuring TCP and ISO-on-TCP connections

  To configure your connection at TCP and ISO-on-TCP, you need to create a DB that contains the data structure of UDT 65 "TCON_PAR." This data structure contains all parameters you need to establish the connection. You need to create such a data structure for each connection, and you can also organize it in a global DB.

  Connection parameter CONNECT of FB 65 "TCON" reports the address of the corresponding connection description to the user program (for example, P#DB100.DBX0.0 byte 64).

- Data blocks for the configuration the local UDP communication access point

  To assign parameters for the local communication access point, create a DB containing the data structure from the UDT 65 "TCON_PAR" This data structure contains the required parameters you need to establish the connection between the user program and the communication level of the operating system

  The CONNECT parameter of the FB 65 "TCON" contains a reference to the address of the corresponding connection description (e.g. P#DB100.DBX0.0 Byte 64).

Note

Setting up the Connection Description (UDT 65)

You have to enter the interface which is to be used for communication in the parameter "local_device_id" in the UDT 65 "TCON_PAR".

This is 16#5 for connection types TCP, UDP, ISO on TCP via the PN interface.

It is 16#0 for connection type ISO on TCP via a CP 443-1.

Establishing a Connection for Communication

- Use with TCP and IS-on-CP

  Both communication partners call FB 65 "TCON" to establish the connection. In your connection configuration, you define which communication partner activates the connection, and which communication partner responds to the request with a passive connection. To determine the number of possible connections, refer to your CPU's technical specifications.

  The CPU automatically monitors and holds the active connection.

  If the connection is broken, for example by line interruption or by the remote communication partner, the active partner tries to reestablish the connection. You do not have to call FB 65 "TCON" again.

  FB 66 "TDISCON" disconnects the CPU from a communication partner, as does STOP mode. To reestablish the connection to have to call FB65 "TCON" again.

- Use with UDP

  Both communication partners call FB 65 "TCON" to set up their local communication access point. This establishes a connection between the user program and operating system's communication level No connection is established to the remote partner.

  The local access point is used to send and receive UDP telegrams.

Disconnecting

- Use with TCP and IS-on-CP

  FB 66 "TDISCON" disconnects the communication connection between CPU and communication partner.

- Use with UDP

  FB 66 "TDISCON" disconnects the local communication access point, i.e., the connection between user program and communication level of operating system is interrupted.

Options for Interrupting the Communication Connection

Events causing interruptions of communication:

- You program the cancellation of connections at FB 66 "TDISCON."
- The CPU goes from RUN to STOP.
- At POWER OFF / POWER ON

Reference

For detailed information on the blocks described earlier, refer to the *STEP 7 Online Help.*

6.7 SNMP Communication Service

Availability

The SNMP communication service is available for CPUs with integrated PROFINET interface and Firmware 5.0 or higher.

Properties

Network diagnostics SNMP (Simple Network Management Protocol) is the standardized protocol for diagnostics of the Ethernet network infrastructure. In the office setting and in automation engineering, devices from many different manufacturers support SNMP on the Ethernet. SNMP-based applications can be operated on the same network in parallel to applications with PROFINET.

Configuration of the SNMP OPC server is integrated in the STEP 7 Hardware Configuration application. Already configured S7 modules from the STEP 7 project can be transferred directly. As an alternative to STEP 7, you can also perform the configuration with the NCM PC (included on the SIMATIC NET CD). All Ethernet devices can be detected by means of their IP address and/or the SNMP protocol (SNMP V1) and transferred to the configuration. The SIMATIC NET SNMP OPC server also provides detection of PROFINET devices using the DCP protocol.

Integration in STEP 7

Applications based on SNMP can be operated on the same network at the same time as applications with PROFINET. A STEP 7 connection is not required for network management with the SNMP protocol.

Diagnostics with SNMP OPC Server in SIMATIC NET

The SNMP OPC server software provides diagnostic and parameter assignment functions for all SNMP devices. The OPC server uses the SNMP protocol to perform data exchange with SNMP devices.

All information can be integrated in OPC-compatible systems, such as the WinCC HMI system. This enables process and network diagnostics to be combined in the HMI system.

Reference

For further information on the SNMP communication service and diagnostics with SNMP, refer to the *PROFINET System Description.*

6.8 PN/IO Address Areas of the CPUs 41x-3PN/DP

Address Areas of the CPUs 41x-3 PN/DP

Table 6-5 PROFINET IO address areas of the CPUs

Address area	CPU 414-3 PN/DP	CPU 416-3 PN/DP
Size of the process image for the respective inputs and outputs	8 KB	16 KB
PROFINET address area, for inputs and outputs	8 KB	8 KB
Number of those in process image for I/Os	Bytes 0 to 255	Bytes 0 to 512

Diagnostics addresses occupy in the input address range 1 byte each for the IO controller, the PN interface and the IO devices (header module at slot 0), and for each module without user data within the device (power module of ET 200S, for example). You can use these addresses, for example, to read module-specific diagnostics data records by calling SFB 52. The diagnostic addresses are specified in your configuration. If you do not specify any diagnostic addresses, STEP 7 assigns these DP diagnostic addresses in ascending order, starting at the highest byte address.

Consistent Data

7

7.1 Basics

Overview

Data that belongs together in terms of its content and describes a process state at a specific point in time is known as consistent data. To maintain consistency, the data should not be changed or updated during processing or transmission.

Example

To ensure that the CPU has a consistent image of the process signals for the duration of cyclic program scanning, the process signals are read from the process image inputs prior to program scanning and written to the process image outputs after the program scanning. Subsequently, during program scanning when the address area "inputs" (I) and "outputs" (O) are addressed, the user program addresses the internal memory area of the CPU on which the image of the inputs and outputs is located instead of directly accessing the signal modules.

SFC 81 "UBLKMOV"

With SFC 81 "UBLKMOV" (uninterruptible block move), you can copy the contents of a memory area (= source area) consistently to a different memory area (= destination area). The copy operation cannot be interrupted by other operating system activities.

SFC 81 "UBLKMOV" enables you to copy the following memory areas:

- Bit memory
- DB contents
- Process Image of Inputs
- Process Image of Outputs

The maximum amount of data you can copy is 512 bytes. Remember the restrictions for the specific CPU as described, for example, in the operations list.

Since copying cannot be interrupted, the interrupt reaction times of your CPU may increase when using SFC 81 "UBLKMOV".

The source and destination areas must not overlap. If the specified destination area is larger than the source area, the function only copies as much data to the destination area as that contained in the source area. If the specified destination area is smaller than the source area, the function only copies as much data as can be written to the destination area.

For information on SFC81, refer to the corresponding online help and to the *System and Standard Functions* manual.

7.2 Consistency for communication blocks and functions

Overview

Using S7-400, the communication jobs are not processed at the scan cycle checkpoint; instead, in fixed time slices during the program cycle.

In the system the byte, word and double word data formats can always be processed consistently, in other words, the transfer or processing of 1 byte, 1 word (= 2 bytes) or 1 double word (= 4 bytes) cannot be interrupted.

If communication blocks (such as SFB^12 "BSEND") are called in the user program, which are only used in pairs (such as SFB 12 "BSEND" and SFB 13 "BRCV") and which share access to data, the access to this data area can be coordinated between themselves, for example, using the "DONE" parameter. Data consistency of the communication areas transmitted locally with a communication block can thus be ensured in the user program.

S7 communication functions such as SFB 14 "GET", SFB 15 "PUT" react differently because no block is needed in the user program of the destination device. In this case the size of data consistency has to be taken into account beforehand during the programming phase.

Access to the Work Memory of the CPU

The communication functions of the operating system access the work memory of the CPU in fixed field lengths. The field size is a variable length up to a maximum of 462 bytes.

7.3 Consistent Reading and Writing of Data from and to DP Standard Slaves/IO Devices

Reading Data Consistently from a DP Standard Slave/IO Device Using SFC 14 "DPRD_DAT"

Using SFC14 "DPRD_DAT" (read consistent data of a DP standard slave) you can consistently read the data of a DP standard slave.

If no error occurred during the data transmission, the read data are entered in the destination area defined by RECORD.

The destination area must be the same length as the one you configured for the selected module with *STEP 7*.

By invoking SFC14 you can only access the data of one module / DP ID at the configured start address.

For information on SFC14, refer to the corresponding online help and to the *System and Standard Functions* manual

Writing Data Consistently to a DP Standard Slave/IO Device Using SFC 15 "DPWR_DAT"

Using SFC 15 "DPWR_DAT" (write consistent data to a DP standard slave) you can consistently write data to the DP standard slave or IO device addressed in the RECORD.

The source area must be the same length as the one you configured for the selected module with *STEP 7*.

Upper Limit for the Transmission of Consistent User Data to a DP Slave

The PROFIBUS DP standard defines the upper limit for the transmission of consistent user data to a DP slave. For this reason a maximum of 64 words = 128 bytes of user data can be consistently transferred in a block to the DP slave.

During the configuration you can determine the size of the consistent area. You can set a maximum length of consistent data at 64 words = 128 bytes in the special identification format (SKF) (128 bytes for inputs and 128 bytes for outputs); the data block size cannot exceed this.

This upper limit only applies to pure user data. Diagnostics and parameter data are regrouped into full records and therefore always transferred consistently.

In the general identification format (AKF) the maximum length of consistent data can be set at 16 words = 32 bytes (32 bytes for inputs and 32 bytes for outputs); the data block size cannot exceed this.

Note in this context that a CPU 41x in a general environment acting as a DP slave on a third-party master (connection defined by GSD) has to be configured with the general identification format. The transfer memory of a CPU 41x acting as a DP slave to the PROFIBUS DP can therefore be a maximum of 16 words = 32 bytes.

For information on SFC 15, refer to the corresponding online help and to the *System and Standard Functions* manual.

Note

The PROFIBUS DP standard defines the upper limit for the transmission of consistent user data. Typical DP standard slaves adhere to this upper limit. In older CPUs (<1999) there are restrictions in the transmission of consistent user data depending on the CPU. For these CPUs you can determine the maximum length of the data which the CPU can consistently read and write to and from the DP standard in the respective technical specifications under the index entry "DP Master – User data per DP slave". Newer CPUs are capable of exceeding the value for the amount of data that a DP standard slave can send and receive.

Upper Limit for the Transmission of Consistent User Data to a IO Device

There is a 255 bytes upper limit for the transmission of consistent user data on an IO device. Even when more than 255 bytes can be transmitted on an IO device, only a maximum of 255 bytes can be consistently transmitted.

Consistent Data Access without the Use of SFC 14 or SFC 15

Consistent data access of > 4 bytes without using SFC 14 or SFC 15 is possible for the CPUs described in this manual. The data area of a DP slave or IO devices that should transfer consistently is transferred to a process image partition. The information in this area is therefore always consistent. You can subsequently use load/transfer commands (such as L IW 1) to access the process image. This is an especially convenient and efficient (low runtime load) way to access consistent data. This allows efficient integration and configuration of drives or other DP slaves, for example.

An I/O access error does **not** occur with direct access (e.g. L PIW or T PQW).

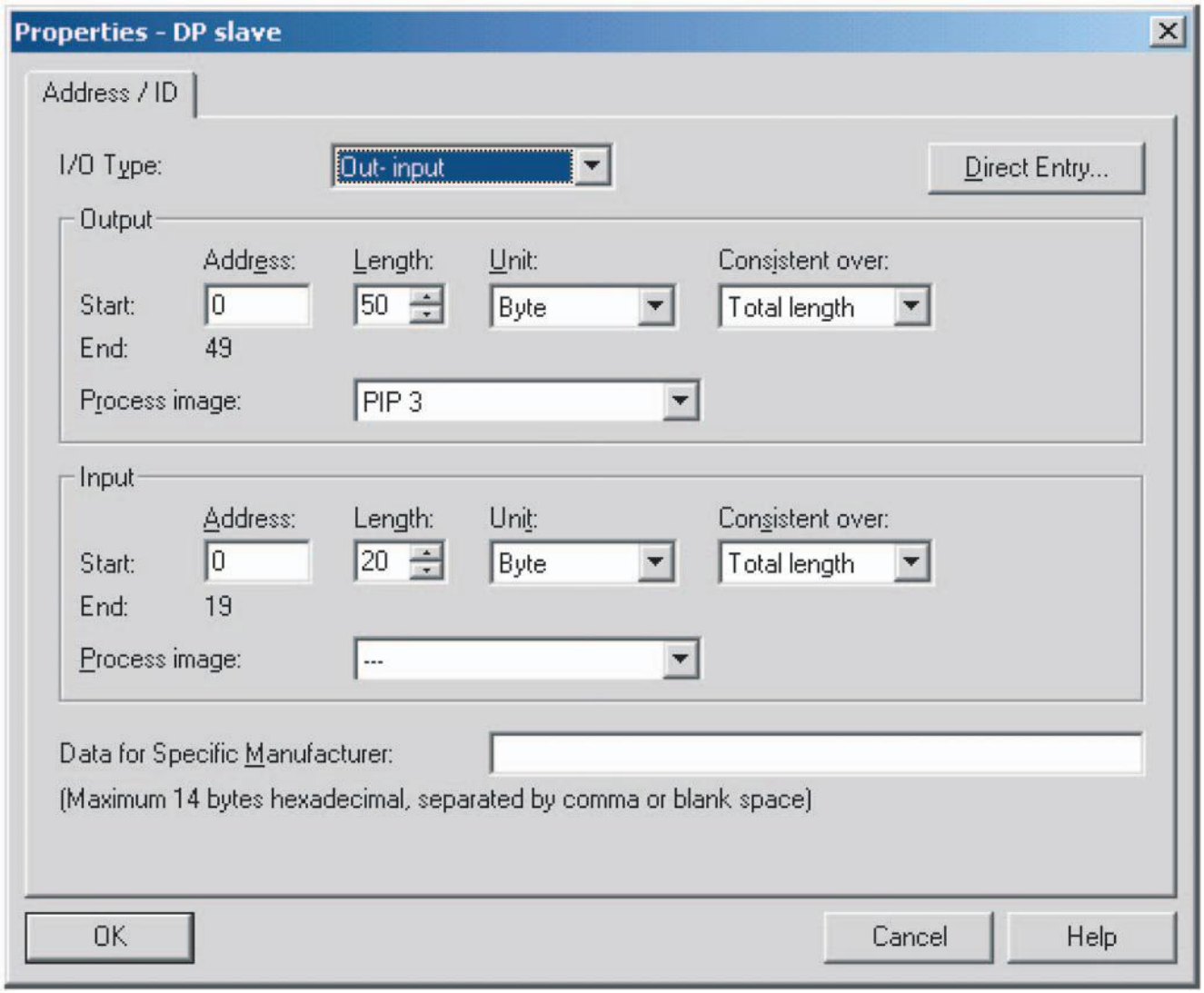
The following is important for converting from the SFC14/15 method to the process image method:

- SFC 50 "RD_LGADR" outputs another address area with the SFC 14/15 method as with the process image method.
- PROFIBUS DP via Interface interface:
  When converting from the SFC14/15 method to the process image method, it is not recommended to use the system functions and the process image at the same time. Although the process image is updated when writing with the system function SFC15, this is not the case when reading. In other words, the consistency between the process image values and the values of the system function SFC14 is not ensured.
- PROFIBUS-DP via CP 443-5 Extended:
  If you are using a CP 443-5 ext, the simultaneous use of SFC14/15 and the process image results in the following errors, you cannot read/write into the process image and/or you can no longer read/write with SFC 14/15.

Example:

The following example (of the process image partition 3 "TPA 3") shows such a configuration in HW Config:

- TPA 3 at output: These 50 bytes are stored consistent in the process image partition 3 (pull-down list "Consistent over -> entire length") and can therefore be read through the normal "load input xy" commands.
- Selecting "Process Image Partition -> ---" under input in the pull-down menu means: do not store in a process image. Then the handling can only be performed using the system functions SFC14/15.



Storage Concept and Startup Types

8

8.1 Overview of the memory concept of S7-400 CPUs

Organization of Memory Areas

The memory of the S7 CPUs can be divided into the following areas:

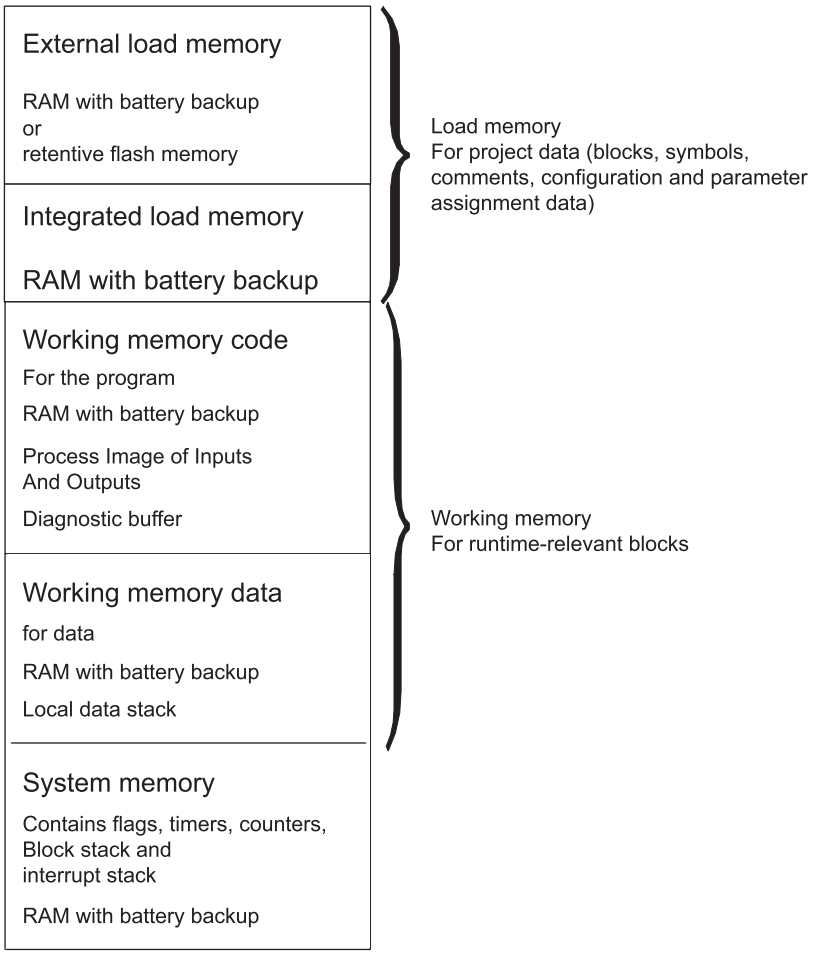


Figure 8-1 Memory areas of the S7-CPUs

Important note for CPUs with selectable allocation of the work memory

If you change the work memory allocation by modifying parameters, this work memory is reorganized when you load system data into the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

The usable size of the working memory for logic or data blocks is changed when loading the system data if you change the following parameters:

- Size of the process image (byte-oriented; in the "Cycle/Clock Memory" tab)
- Communication resources (S7-400 only; "Memory" tab)
- Size of the diagnostic buffer ("Diagnostics/Clock" tab)
- Number of local data for all priority classes ("Memory" tab)

Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory on the CPU, you must take into consideration the following memory requirements when assigning parameters:

Table 8-1 Memory requirements

Parameters	Required working memory	In code/data memory
Size of the process image (inputs)	12 bytes per byte in the process input image	Code memory
Size of the process image (outputs)	12 bytes per byte in the process output image	Code memory
Communication resources (communication jobs)	72 bytes per communication job	Code memory
Size of the diagnostic buffer	32 bytes per entry in the diagnostic buffer	Code memory
Quantity of local data	1 byte per byte of local data	Data memory

Memory Types in S7-400 CPUs

- Load memory for project data, such as blocks, configuration and parameter assignment data, including symbols and comments as of version 5.1.
- Work memory for the runtime-relevant blocks (logic blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as bit memory, timers and counters. System memory also contains the block stack

- System memory of the CPU also makes temporary memory available (local data stack, diagnostic buffer and communication resources) that is assigned to the program for the temporary data of a called block. These data are only valid as long as the block is active.

  By changing the default values for the process image, local data, diagnostic buffer and communication resources (see object properties of the CPU in HW Config), you can influence the work memory available to the runtime-relevant blocks.

Notice

Please note the following if you expand the process image of a CPU. Make sure that you configure the modules that can only be operated above the process image in such a way that they are also positioned above the expanded process image. This applies, in particular, to IP and WF modules that you operate in the S5 adapter casing in an S7-400.

Flexible Memory Capacity

- Work memory:

  The capacity of the work memory is determined by selecting the appropriate CPU from the graded range of CPUs.

- Load memory:

  The integrated load memory is sufficient for small and medium-sized programs.

  The load memory can be increased for larger programs by inserting the RAM memory card.

  Flash memory cards are also available to ensure that programs are retained in the event of a power failure even without a backup battery. Flash memory cards can also be used (more than 4 MB, at CPUs with FW Version 5.0 more than 8 MB) to send and run operating system updates.

Backup

- The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.

8.2 Overview of the startup scenarios for S7-400 CPUs

Cold Start

- During a cold restart, all data (process image, bit memory, timers, counters and data blocks) are reset to the start values stored in the program (load memory), irrespective of whether they were configured as retentive or non-retentive.
- Program execution is restarted at the beginning (startup OB or OB1).

Restart (Warm Restart)

- A warm restart resets the process image and the non-retentive flags, timers, times and counters.

  Retentive flags, times and counters retain their last valid value.

  All data blocks assigned the "Non Retain" attribute are reset to the load values. The remaining data blocks retain their last valid value.
- Program execution is restarted at the beginning (startup OB or OB 1).
- After a power supply interruption, the warm restart function is only available in backup mode.

Hot restart

- When a hot restart is performed, all data and the process image retain their last valid value.
- Program execution is resumed at the breakpoint.
- The outputs do not change their status until the current cycle is completed.
- After a power supply interruption, the hot restart function is only available in backup mode.

Cycle and Response Times of the S7-400

9

9.1 Cycle time

Definition of the Cycle Time

The cycle time represents the time that an operating system needs to execute a program, that is, one OB 1 cycle, including all program sections and system activities interrupting this cycle.

This time is monitored.

Time-Sharing Model

Cyclic program scanning, and thus also processing of the user program, is performed in time slices. So that you can better appreciate these processes, we will assume in the following that each time slice is exactly 1 ms long.

Process Image

The process signals are read or written prior to program scanning so that a consistent image of the process signals is available to the CPU for the duration of cyclic program scanning. Then the CPU does not directly access the signal modules during program scanning when the address area "inputs" (I) and "outputs" (O) are addressed, but addresses instead the internal memory area of the CPU on which the image of the inputs and outputs is located.

The Cyclic Program Scanning Process

The following table and figure illustrate the phases of cyclic program scanning.

Table 9-1 Cyclic program processing

Step	Process
1	The operating system starts the scan cycle monitoring time.
2	The CPU writes the values from the process-image output table in the output modules.
3	The CPU reads out the status of the inputs at the input modules and updates the process-image input table.
4	The CPU processes the user program in time slices and performs the operations specified in the program.
5	At the end of a cycle, the operating system executes pending tasks, such as the loading and clearing of blocks.
6	The CPU then goes back to the beginning of the cycle after the configured minimum cycle time, as necessary, and starts cycle time monitoring again.

Parts of the Cycle Time

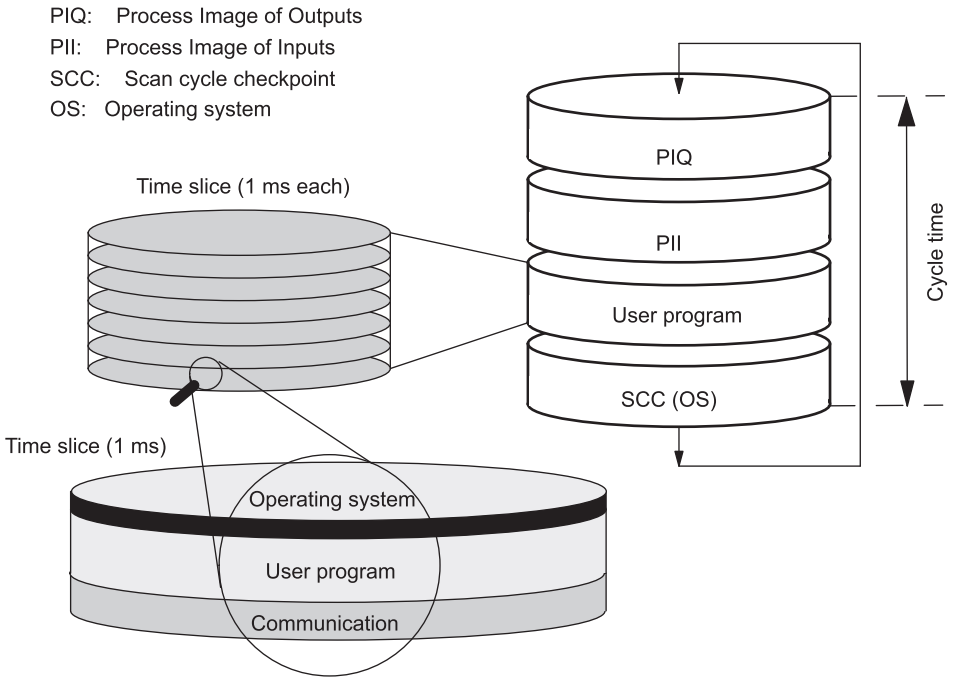


Figure 9-1 Parts and Composition of the Cycle Time

9.2 Cycle Time Calculation

Increasing the Cycle Time

Basically, you should note that the cycle time of a user program is increased by the following:

- Time-driven interrupt processing
- Hardware interrupt processing
- Diagnostics and error handling
- Communications via the MPI, PROFINET interface and CPs connected automation-system internally
  (for example, Ethernet, PROFIBUS DP); included in the communication load
- Special functions such as control and monitoring of tags or block status
- Transfer and clearance of blocks, compression of the user program memory
- Internal memory test

Influencing factors

The following table indicates the factors that influence the cycle time.

Table 9-2 Factors that Influence the Cycle Time

Factors	Remarks
Transfer time for the process-image output table (PIQ) and the process-image input table (PII)	... See table "Portions of the process image transfer time"
User program execution time	... is calculated from the execution times of the different instructions, see *S7-400 Instruction List*.
Operating system scan time at the scan cycle checkpoint	... See table "Operating system scan time at the scan cycle checkpoint"
Increase in the cycle time through communications	You set the maximum permissible cycle load expected for communication in % in *STEP 7*, see manual *Programming with STEP 7*.
Impact of interrupts on the cycle time	Interrupt can interrupt the user program at any time. ... See table "Increase in cycle time by nesting interrupts"

Process Image Updating

The table below shows the CPU times for process image updating (process image transfer time). The times listed in the table are "ideal values" that may be increased by the occurrence of interrupts and by CPU communications.

The transfer time for process image updating is calculated as follows

C + portion in central controller (from row A of the following table)
+ portion in the expansion rack with local connection (from row B)
+ portion in the expansion rack with remote connection (from row C)
+ portion over integrated DP interface (from row D)
+ portion of consistent data over integrated DP interface (from row E1)
+ portion of consistent data over external DP interface (from row E2)

= Transfer time for the process image update

The tables below show the individual portions of the transfer time process image updating (process image transfer time). The times listed in the table are "ideal values" that may be increased by the occurrence of interrupts and by CPU communications.

Table 9-3 Portions of the process image transfer time

	Portions	**CPU 414**	**CPU 416**
	n = number of bytes in the process image		
C	Base load	7 µs	5 µs
O	In the central rack *)	n * 1.8 µs	n * 1.75 µs
B	In the expansion rack with local connection *)	n * 5.5 µs	n * 5.4 µs
C	In the expansion rack with remote connection *) **) Reading Writing	 n * 12 µs n * 11 µs	 n * 12 µs n * 11 µs
D 1	In the DP area for the integrated DP interface	n * 0.5 µs	n * 0.45 µs
D 2	In the DP area for the external DP interface CP 443-5 extended	n * 2.5 µs	n * 2.4 µs
E 1	Consistent data in the process image for the integrated DP interface	n * 0.45 µs	n * 0.3 µs
E 2	Consistent data in the process image for the external DP interface (CP 443-5 extended)	n * 2.0 µs	n * 2.0 µs
F 1	In the PN/IO area for the integrated interface	n * 5.6 µs	n * 5.6 µs
F 2	In the PN/IO area for the external interface CP 443-1 EX 41	n * 3.1 µs	n * 2.8 µs

*In the case of I/O modules that are plugged into the central rack or an expansion rack, the specified value contains the runtime of the I/O module

**Measured with the IM 460-3 and IM 461-3 with a connection length of 100 m

Operating System Scan Time at the Scan Cycle Checkpoint

The table below lists the operating system scan times at the scan cycle checkpoint of the CPUs.

*In the case of I/O modules that are plugged into the central rack or an expansion rack, the specified value contains the runtime of the I/O module

**Measured with the IM 460-3 and IM 461-3 with a connection length of 100 m

*** The areas set in HW Config that are written once to the I/O or are read once from the I/O and are therefore consistent.

Table 9-4 Operating System Scan Time at the Scan Cycle Checkpoint

Process	CPU 414	CPU 416
Scan cycle control at the SCC	160 µs to 239 µs Ø 168 µs	104 µs to 163 µs Ø 109 µs

Increase in cycle time by nesting interrupts

Table 9-5 Increase in cycle time by nesting interrupts

CPU	Hardware interrupt	Diagnostic interrupt	Time-of-day Interrupt	Time-delay interrupt	Cyclic interrupt	Programming / PI/O access error
CPU 414	314 µs	308 µs	237 µs	217 µs	210 µs	84 µs / 84 µs
CPU 416	213 µs	232 µs	139 µs	135 µs	141 µs	55 µs / 56 µs

You have to add the program execution time at the interrupt level to this increase.

If several interrupts are nested, their times must be added together.

9.3 Different cycle times

Fundamentals

The length of the cycle time (T_{cyc}) is not identical in each cycle. The following figure shows different cycle times, T_{cyc1} and T_{cyc2}. T_{cyc2} is longer than T_{cyc1}, because the cyclically scanned OB 1 is interrupted by a time-of-day interrupt OB (here, OB10).

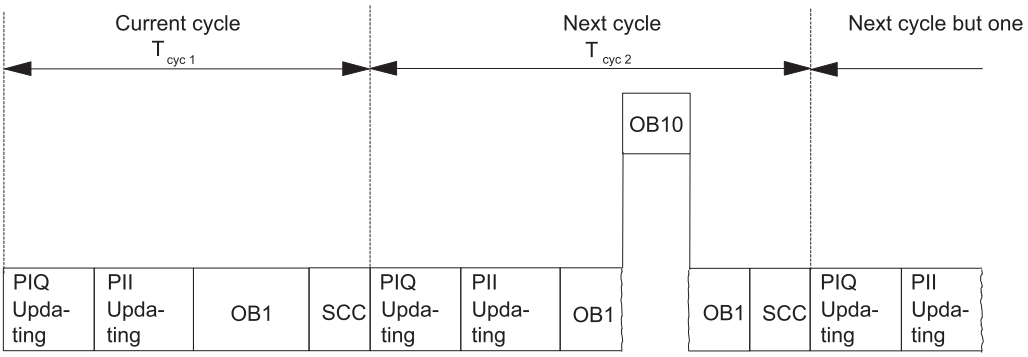


Figure 9-2 Different cycle times

Fluctuation of the block processing time (e.g. OB 1) may also be a factor causing cycle time fluctuation, due to:

- Conditional commands
- Conditional block calls
- Different program paths,
- Loops, etc.

Maximum Cycle Time

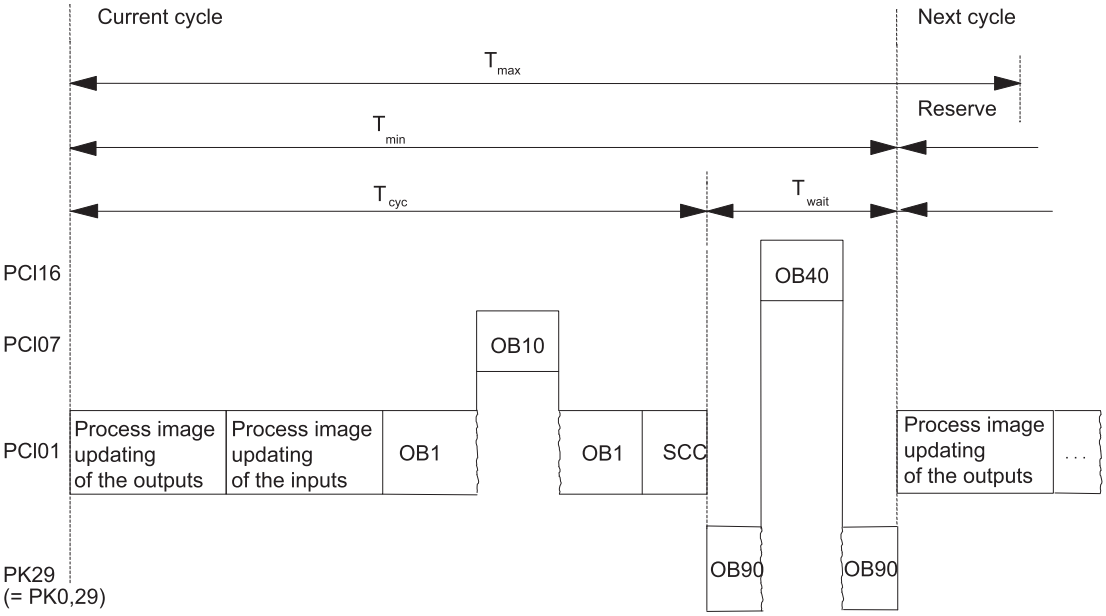
You can modify the default maximum cycle time in STEP 7 (cycle monitoring time). When this time has expired, OB 80 is called. In OB 80 you can specify how the CPU is to react to time errors. If you do not retrigger the cycle time with SFC43, OB 80 doubles the cycle time at the first call. In this case, the CPU goes to STOP at the second call of OB 80.

If there is no OB 80 in the CPU memory, the CPU goes to STOP.

Minimum Cycle Time

You can set a minimum cycle time for a CPU in STEP 7. This is appropriate in the following cases:

- you want the intervals of time between the start of program scanning of OB1 (free cycle) to be roughly of the same length.
- updating of the process images would be performed unnecessarily often with too short a cycle time.
- You want to process a program with the OB 90 in the background.



Tmin = the adjustable minimum cycle time
Tmax = the adjustable maximum cycle time
Tcyc = the cycle time
Twait = the difference between Tmin and the actual cycle time; in this time, any interrupts that occur, the background OB and the SCC tasks can be processed.
PCI = priority class

Figure 9-3 Minimum cycle time

The actual cycle time is the sum of T_{cyc} and T_{wait}. It is always greater than or equal to T_{min}.

9.4 Communication Load

Overview

The CPU operating system continually makes available to communications the percentage you configured for the overall CPU processing performance (time sharing). Processing performance not required for communication is made available to other processes.

In the hardware configuration, you can set the load due to communications between 5% and 50%. By default, the value is set to 20%.

This percentage should be regarded as an average value, in other words, the communications component can be considerably greater than 20% in a time slice. On the other hand, the communications component in the next time slice is only a few or zero percent.

This fact is also expressed by the following equation:

$$\text{Actual cycle time} = \text{Cycle time} \times \frac{100}{100 - \text{"configured communication load in \%"}}$$

Round up the result to the next whole number !

Figure 9-4 Equation: Influence of Communication Load

Data Consistency

The user program is interrupted for communications processing. The interrupt can be executed after any instruction. These communication jobs can modify the program data. This means that the data consistency cannot be guaranteed for the duration of several accesses.

The section *Consistent Data* provides more information about how to ensure consistency when there is more than one command.

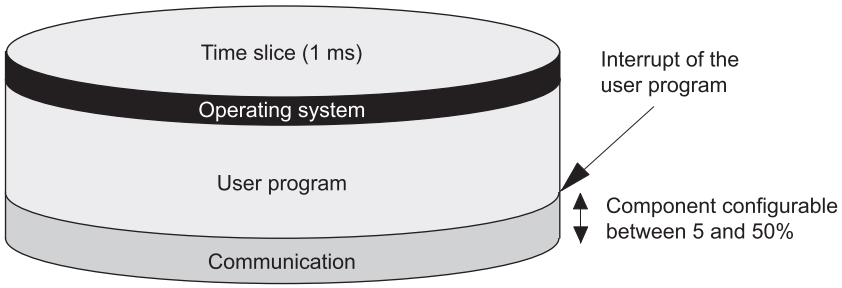


Figure 9-5 Breakdown of a time slice

Of the part remaining, the operating system of the S7-400 requires only a negligibly small amount for internal tasks.

Example: 20% communication load

You have configured a communication load of 20% in the hardware configuration.

The calculated cycle time is 10 ms.

A 20% communication load means that, on average, 200 µs and 800 µs of the time slice remain for communications and the user program, respectively. The CPU therefore requires 10 ms / 800 µs = 13 time slices to process one cycle. This means that the actual cycle time is 13 times a 1 ms time slice = 13 ms, if the CPU fully utilizes the configured communication load.

This means that 20% communications do not increase the cycle linearly by 2 ms but by 3 ms.

Example: 50 % communication load

You have configured a communication load of 50% in the hardware configuration.

The calculated cycle time is 10 ms.

This means that 500 µs of each time slice remain for the cycle. The CPU therefore requires 10 ms / 500 µs = 20 time slices to process one cycle. This means that the actual cycle time is 20 ms if the CPU fully utilizes the configured communication load.

A 50% communication load means that 500 µs of the time slice remain for communication and 500 µs for the user program. The CPU therefore requires 10 ms / 500 µs = 20 time slices to process one cycle. This means that the actual cycle time is 20 times a 1 ms time slice = 20 ms, if the CPU fully utilizes the configured communication load.

This means that 50% communications do not increase the cycle linearly by 5 ms but by 10 ms.

Dependency of the Actual Cycle Time on the Communication Load

The following figure describes the non-linear dependency of the actual cycle time on the communication load. This example uses a cycle time of 10 ms.

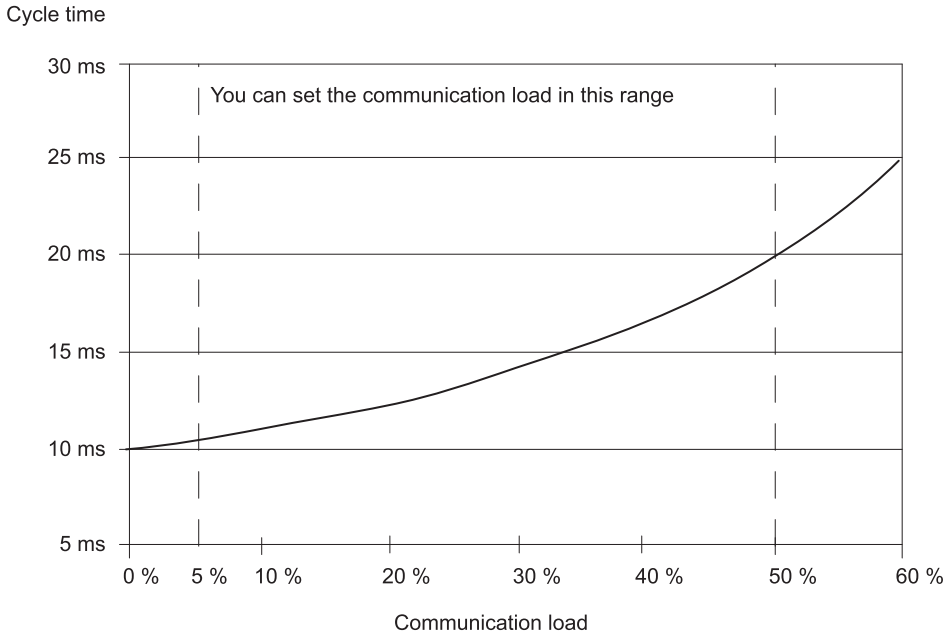


Figure 9-6 Dependency of the Cycle Time on the Communication Load

Further Effect on the Actual Cycle Time

Due to the increase in the cycle time as a result of the communications component, even more asynchronous events occur, from a statistical point of view, within an OB 1 cycle than, say, interrupts. This also increases the OB 1 cycle. This extension depends on the number of events that occur per OB 1 cycle and the time required to process these events.

Notes

- Check the effects of a change of the value for the parameter "Cycle load due to communications" in system operation.
- The communication load must be taken into account when you set the maximum cycle time, since time errors will occur if it is not.

Recommendations

- If possible, apply the default value.
- Use a larger value only if the CPU is being used primarily for communication purposes and the user program is non-time-critical. In all other cases select a smaller value.

9.5 Reaction Time

Definition of the Response Time

The response time is the time from an input signal being detected to changing an output signal linked to it.

Variation

The actual response time is somewhere between a shortest and a longest response time. For configuring your system, you must always reckon with the longest response time.

The shortest and longest response times are analyzed below so that you can gain an impression of the variation of the response time.

Factors

The response time depends on the cycle time and on the following factors:

- Delay in the inputs and outputs
- Additional DP cycle times on the PROFIBUS-DP network
- Execution of the user program

Delay in the Inputs and Outputs

Depending on the module, you must heed the following time delays:

• For digital inputs:	The input delay time
• For digital inputs with interrupt capability:	The input delay time + module-internal preparation time
• For digital outputs	Negligible delay times
• For relay outputs:	Typical delay times of 10 ms to 20 ms. The delay of the relay outputs depends, among other things, on the temperature and the voltage.
• For analog inputs:	Analog input cycle time
• For analog outputs:	Response time of analog outputs

The time delays can be found in the technical specifications of the signal modules.

DP Cycle Times on the PROFIBUS-DP Network

If you have configured your PROFIBUS-DP network with **STEP 7**, then **STEP 7** will calculate the typical DP cycle time that must be expected. You can then have the DP cycle time of your configuration displayed for the bus parameters on the programming device.

The following figure will provide you with an overview of the DP cycle time. We assume in this example that each DP slave has 4 bytes of data on average.

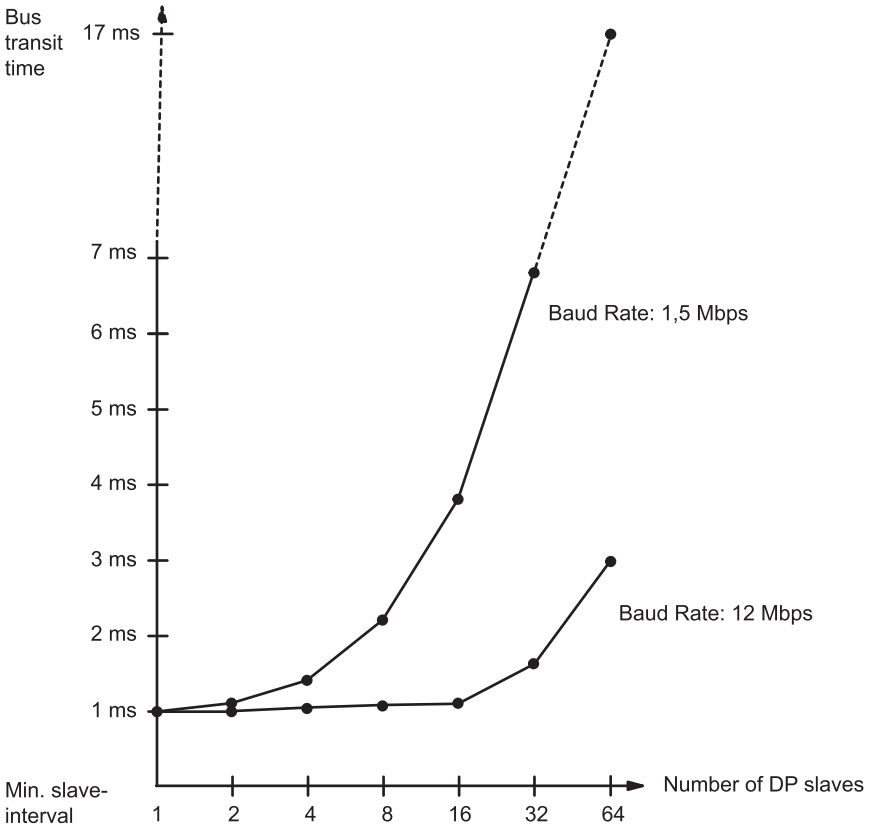


Figure 9-7 DP Cycle Times on the PROFIBUS-DP Network

With multi-master operation on a PROFIBUS-DP network, you must make allowances for the DP cycle time at each master. That is, you will have to calculate the times for each master separately and then add up the results.

Update Cycle in PN/IO

An overview of the duration of the update cycle depending on the number IO devices contained in the cycle in the following figure.

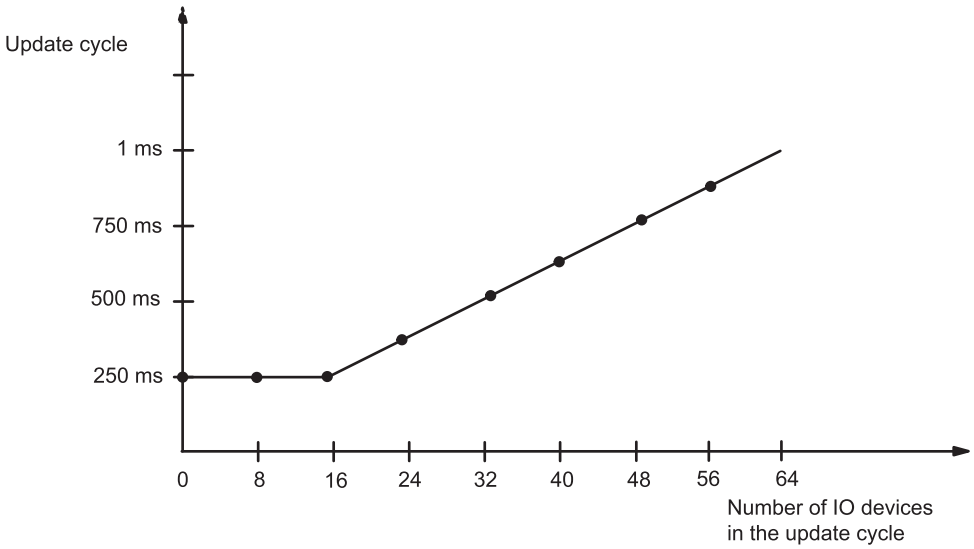


Figure 9-8 Update cycle

Shortest Response Time

The following figure illustrates the conditions under which the shortest response time can be achieved.

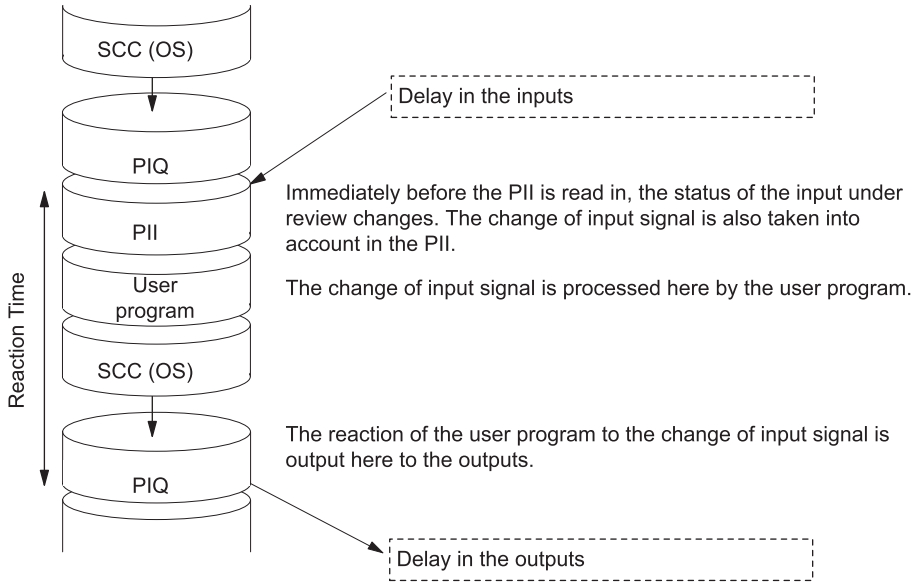


Figure 9-9 Shortest response time

Calculation

The (shortest) response time is made up as follows:

- 1 x process image transfer time for the inputs +
- 1 x process image transfer time for the outputs +
- 1 x program processing time +
- 1 × operating system processing time at the SCC +
- Delay in the inputs and outputs

The result is equivalent to the sum of the cycle time plus the I/O delay times.

Note

If the CPU and signal module are not in the central rack, you have to add double the runtime of the DP slave frame (including processing in the DP master).

Longest Response Time

The following figure shows you how the longest response time results.

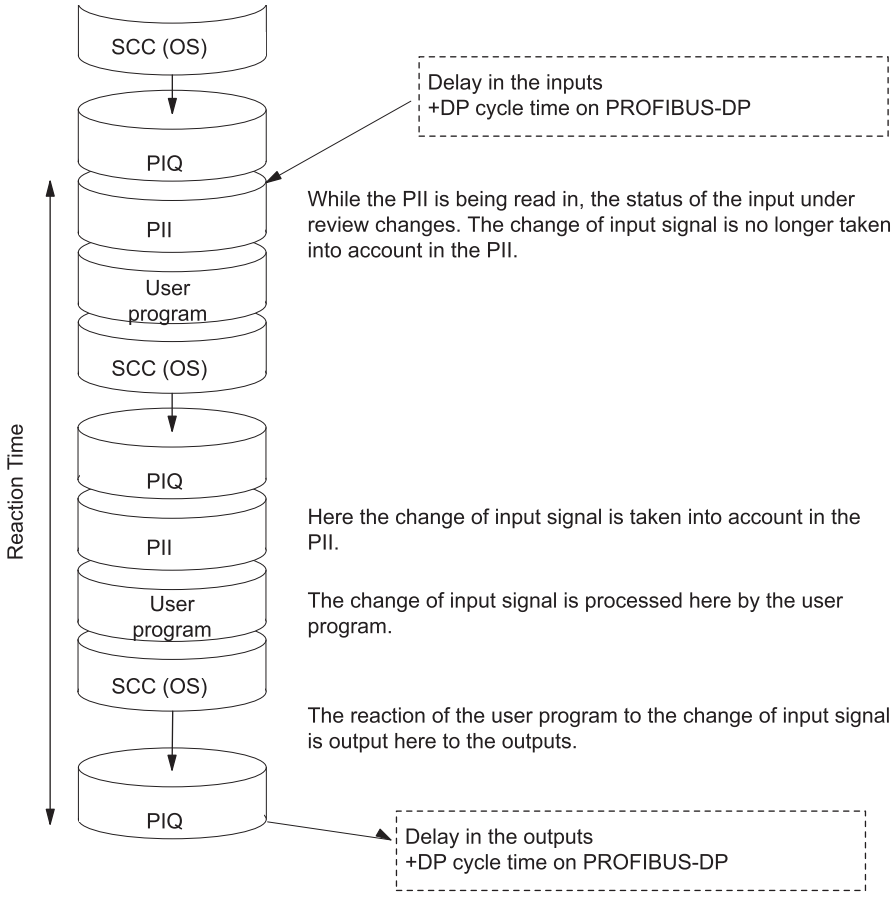


Figure 9-10 Longest response time

Calculation

The (longest) response time is made up as follows:

- 2 x process image transfer time for the inputs +
- 2 x process image transfer time for the outputs +
- 2 × operating system processing time +
- 2 x program processing time +
- 2 x runtime of the DP slave frame (including processing in the DP master) +
- Delay in the inputs and outputs

This is equivalent to the sum of twice the cycle time and the delay in the inputs and outputs plus twice the DP cycle time.

I/O Direct Accesses

You can reach faster response times with direct access to the I/O in your user program. For example, you can partially circumvent the response times as described above by using one of the following commands:

- L PIB
- T PQW

Reducing the Response Time

In this way the maximum response time is reduced to the following components:

- Delay in the inputs and outputs
- Runtime of the user program (can be interrupted by high-priority interrupt handling)
- Runtime of direct accesses
- Twice the bus transit time of DP

The following table lists the execution times of direct accesses by the CPU to I/O modules. The times shown are "ideal values".

Table 9-6 Reducing the Response Time

Access mode	CPU 414	CPU 416
I/O module		
Read byte	2.6 µs	2.5 µs
Read word	4.2 µs	4.0 µs
Read double word	7.2 µs	7.1 µs
Write byte	2.3 µs	2.2 µs
Write word	3.6 µs	3.4 µs
Write double word	6.2 µs	5.9 µs
Expansion rack with local connection		
Read byte	6,0 µs	5,7 µs
Read word	11,0 µs	10,8 µs
Read double word	21,0 µs	20,8 µs
Write byte	5,4 µs	5,4 µs
Write word	10,1 µs	10,0 µs
Write double word	19,5 µs	19,4 µs
Read byte in the expansion rack with remote connection		
Read byte	11,3 µs	11,3 µs
Read word	22,8 µs	22,8 µs
Read double word	45,9 µs	45,9 µs
Write byte	10,8 µs	10,8 µs
Write word	21,9 µs	21,9 µs
Write double word	44,0 µs	44,0 µs

The specified times are merely CPU processing times and apply, unless otherwise stated, to signal modules in the central rack.

Note

You can similarly achieve fast response times by using hardware interrupts; refer to the section on the interrupt response time.

9.6 Calculating cycle and reaction times

Cycle Time

1. Using the Instruction List, determine the runtime of the user program.
2. Calculate and add the transfer time for the process image. You will find approximate values in the table "Portions of the process image transfer time".
3. Add to it the processing time at the scan cycle checkpoint. You will find approximate values in the table "Portions of the process image transfer time".

The result you achieve is the **cycle time**.

Increasing the Cycle Time with Communication and Interrupts

1. The next step is to multiply the result by the following factor:

$$\frac{100}{100 - \text{"configured communication load in \%"}}$$

2. Using the Instruction List, calculate the runtime of the program sections that hardware interrupts. Add to it the relevant value from the table "Increase in cycle time by nesting interrupts".

   Multiply this value by the factor from step 1.
   Add this value to the theoretical cycle time as often as the interrupt is triggered or is expected to be triggered during the cycle time.

The result you obtain is approximately the **actual cycle time**. Make a note of the result.

Table 9-7 Example of Calculating the Response Time

Shortest response time	Longest response time
6. Then, calculate the delays in the inputs and outputs and, if applicable, the DP cycle times on the PROFIBUS DP network.	6. Multiply the actual cycle time by a factor of 2.
	7. Then, calculate the delays in the inputs and outputs and the DP cycle times on the PROFIBUS DP network.
7. The result you obtain is the **shortest response time**.	8. The result you obtain is the **longest response time**.

9.7 Examples of Calculating the Cycle Time and Reaction Time

Example I

You have installed an S7-400 with the following modules in the central rack:

- One CPU 414-2
- 2 digital input modules SM 421; DI 32xDC 24 V (4 bytes each in the PI)
- 2 digital output modules SM 422; DO 32xDC 24 V/0.5A (4 bytes each in the PI)

User Program

According to the Instruction List, your user program has a runtime of 12 ms.

Cycle Time Calculation

The cycle time for the example results from the following times:

- Process image transfer time

  Process image: 7 µs + 16 bytes×1.5 µs = approx. **0.042 ms**
- Operating system runtime at scan cycle checkpoint:
  approx. **0.17 ms**

The cycle time for the example results from the sum of the times listed:

Cycle time = 12.00 ms + 0.042 ms + 0.17 ms **= 12.21 ms.**

Calculation of the Actual Cycle Time

- Allowance of communication load (default value: 20 %):
  12.21 ms x 100 / (100-20) **= 15.26 ms.**
- There is no interrupt handling.

The actual rounded cycle time is therefore **15.3 ms.**

Calculation of the Longest Response Time

- Longest response time
  15.3 ms * 2 **= 30.6 ms.**
- The delay in the inputs and outputs is negligible.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- There is no interrupt handling.

The longest rounded response time is therefore **31 ms.**

Example II

You have installed an S7-400 with the following modules:

- One CPU 414-2
- 4 digital input modules SM 421; DI 32xDC 24 V (4 bytes each in the PI)
- 3 digital output modules SM 422; DO 16xDC 24 V/2A (2 bytes each in the PI)
- 2 analog input modules SM 431; AI 8x13Bit (not in PI)
- 2 analog output modules SM 432; AO 8x13Bit (not in PI)

CPU Parameters

The CPU has been assigned parameters as follows:

- Cycle load due to communications: 40%

User Program

According to the Instruction List, the user program has a runtime of 10.0 ms.

Cycle Time Calculation

The theoretical cycle time for the example results from the following times:

- Process image transfer time

  Process image: 7 µs + 22 bytes×1.5 µs = approx. **0.047 ms**
- Operating system runtime at scan cycle checkpoint:
  approx. **0.17 ms**

The cycle time for the example results from the sum of the times listed:

Cycle time = 10.0 ms + 0.047 ms + 0.17 ms **= 10.22 ms.**

Calculation of the Actual Cycle Time

- Allowance of communication load:
  10.22 ms x 100 / (100-40) **= 17.0 ms.**

  Every 100 ms, a time-of-day interrupt is triggered with a runtime of 0.5 ms.
  The interrupt can be triggered a maximum of once during a cycle:

  0.5 ms + 0.24 ms (from table " Increase in cycle time by nesting interrupts") **= 0.74 ms.**

  Allowance for communication load:

  0.74 ms x 100 / (100-40) **= 1.23 ms.**
- 17.0 ms + 1.23 ms **= 18.23 ms.**

The actual cycle time is therefore **18.23 ms** taking into account the time slices.

Calculation of the Longest Response Time

- Longest response time
  18.23 ms * 2 **= 36.5 ms.**
- Delays in the inputs and outputs
  - The digital input module SM 421; DI 32xDC 24 V has an input delay of not more than **4.8 ms** per channel
  - The digital output module SM 422; DO 16xDC 24 V/2A has a negligible output delay.
  - The analog input module SM 431; AI 8x13Bit was assigned parameters for 50 Hz interference frequency suppression. This results in a conversion time of 25 ms per channel. Since 8 channels are active, a cycle time of **200 ms** results for the analog input module.
  - The analog output module SM 432; AO 8x13-bit was programmed for the measuring range of 0 to 10V. This results in a conversion time of 0.3 ms per channel. Since 8 channels are active, a cycle time of 2.4 ms results. The settling time for the resistive load of 0.1 ms must still be added. The result is a response time of **2.5 ms** for an analog output.
- All the components are plugged into the central rack; DP cycle times do not therefore have to be taken into account.
- Case 1: When a digital signal is read in, an output channel of the digital output module is set. This produces a response time of:

  Response time = 36.5 ms + 4.8 ms = **41.3 ms**.
- Case 2: An analog value is read in and an analog value output. This produces a response time of:

  Response time = 36.5 ms + 200 ms + 2.5 ms **= 239.0 ms**.

9.8 Interrupt Reaction Time

Definition of the Interrupt Response Time

The interrupt response time is the time from when an interrupt signal first occurs to calling the first instruction in the interrupt OB.

General rule: Interrupts having a higher priority take precedence. This means that the interrupt response time is increased by the program processing time of the higher priority interrupt OBs and interrupt OBs with the same priority that have not yet been processed (queue).

Note

Read and write jobs with the maximum amount of data (approx. 460 bytes), interrupt response times can be delayed.
When interrupts are transferred between a CPU and DP master, only a diagnostic **or** hardware interrupt can be currently reported at any time from a DP chain.

Calculation

Table 9-8 Calculating the Interrupt Response Time

Minimum interrupt response time of the CPU + minimum interrupt response time of the signal modules + DP cycle time on PROFIBUS-DP _____ = Shortest response time	Maximum interrupt response time of the CPU + maximum interrupt response time of the signal modules + 2 * DP cycle time on PROFIBUS-DP _____ = Longest response time

Hardware Interrupt and Diagnostic Interrupt Response Times of CPUs

Table 9-9 Hardware Interrupt and Diagnostic Interrupt Response Times; Maximum Interrupt Response Time Without Communication

CPU	Process interrupt response times		Diagnostic interrupt response times		Asynchronous error (OB 85 in process image update)
	Min.	Max.	Min.	Max.	
414	205 µs	218 µs	204 µs	238 µs	164 µs
416	139 µs	147 µs	138 µs	145 µs	107 µs

Increasing the maximum interrupt response time with communication

The maximum interrupt response time increases when communication functions are active. The increase is calculated with the following equation:

tv = 100 µs + 1000 µs x n%

where n = cycle load from communication

Signal Modules

The hardware interrupt response time of the signal modules is made up as follows:

- Digital input modules:

  Hardware interrupt response time = internal interrupt processing time + input delay

  You will find the times in the data sheet of the digital input module concerned.

- Analog input modules:

  Hardware interrupt response time = internal interrupt processing time + conversion time

  The internal interrupt processing time of the analog input modules is negligible. The conversion times can be taken from the data sheet of the analog input module concerned.

The diagnostic interrupt response time of the signal modules is the time which elapses between a diagnostics event being detected by the signal module and the diagnostic interrupt being triggered by the signal module. This time is so small that it can be ignored.

Hardware Interrupt Processing

When the hardware interrupt OB 40 is called, the hardware interrupt is processed. Interrupts with higher priority interrupt hardware interrupt processing, and direct access to the I/O is made when the instruction is executed. When hardware interrupt processing is completed, either cyclic program processing is continued or other interrupt OBs with the same or a lower priority are called and processed.

9.9 Example: Calculating the Interrupt Reaction Time

Parts of the Interrupt Response Time

As a reminder: The hardware interrupt response time comprises the following:

- Hardware interrupt response time of the CPU
- Hardware interrupt response time of the signal module.
- 2 x DP cycle time on PROFIBUS-DP

Example: You have an S7-400 consisting of a CPU 416-2 and 4 digital modules in the central rack. One digital input module is the SM 421; DI 16×UC 24/60 V; with hardware and diagnostic interrupts. In the parameter assignment of the CPU and the SM, you have only enabled the hardware interrupt. You do not require time-driven processing, diagnostics and error handling. You have set an input delay of 0.5 ms for the digital input module. No activities are necessary at the cycle checkpoint. You have set a cycle load caused by communication of 20%.

Calculation

The hardware interrupt response time for the example results from the following times:

- Hardware interrupt response time of the CPU 416-2: Approx. 0.23 ms
- Extension by communication according to the equation in the table "Hardware interrupt and diagnostic interrupt response times; maximum interrupt response time without communication":

100 µs + 1000 µs x 20 % = 300 µs = 0.3 ms

- Hardware interrupt response time of the SM 421; DI 16xUC 24/60 V:
  - Internal interrupt processing time: 0.5 ms
  - Input delay: 0.5 ms
- Since the signal modules are plugged into the central rack, the DP cycle time on the PROFIBUS-DP is not relevant.

The hardware interrupt response time results from the sum of the listed times:

Hardware interrupt response time = 0.23 ms +0.3 ms + 0.5 ms + 0.5 ms = **approx. 1.53 ms**.

This calculated hardware interrupt response time is the time from a signal being applied across the digital input to the first instruction in OB 40.

9.10 Reproducibility of Time-Delay and Watchdog Interrupts

Definition of "Reproducibility"

Time-delay interrupt:

The deviation with time from the first instruction of the interrupt OB being called to the programmed interrupt time.

Watchdog interrupt:

The variation in the time interval between two successive calls, measures between the first instruction of the interrupt OB in each case.

Reproducibility

The following table contains the reproducibility of time-delay and cyclic interrupts of the CPUs.

Table 9-10 Reproducibility of Time-Delay and Watchdog Interrupts of the CPUs.

Module	Reproducibility	
	Time delay interrupt:	Cyclic interrupt
CPU 414	-182 µs / +185 µs	-25 µs / +26 µs
CPU 416	-210 µs / +206 µs	-16 µs / +18 µs

These times only apply if the interrupt can actually be executed at this time and if not interrupted, for example, by higher-priority interrupts or queued interrupts of equal priority.

9.11 CBA response times

Definition of the Response Time

The response time is the time that it takes a value from the user program of a CPU to reach the user program of a second CPU. This assumes that no time is lost in the user program itself.

Response Time for Cyclic Interconnection

The response time of an interconnection in an S7-400 CPU is composed of the following portions:

- Processing time on the transmitting CPU
- The transmission frequency configured in SIMATIC iMap (fast, medium or slow)
- Processing time on the receiving CPU

You have specified a value for the transmission frequency suited to your plant during the configuration with SIMATIC iMap. Faster or slower response times can occur because the data transmission to the user program is performed asynchronously. Therefore, check the achievable response time during commissioning and change the configuration as required.

Measurements for Cyclic Interconnections in an Example Configuration

To be able to estimate the achievable CBA response time better, consider the following measurements.

The processing times on the transmitting CPU and the receiving CPU basically depend on the sum of the input and output interconnections and the amount of data on them. The following figure shows this relationship using two examples for transmitting 600 bytes and 9600 bytes to a varying number of interconnections:

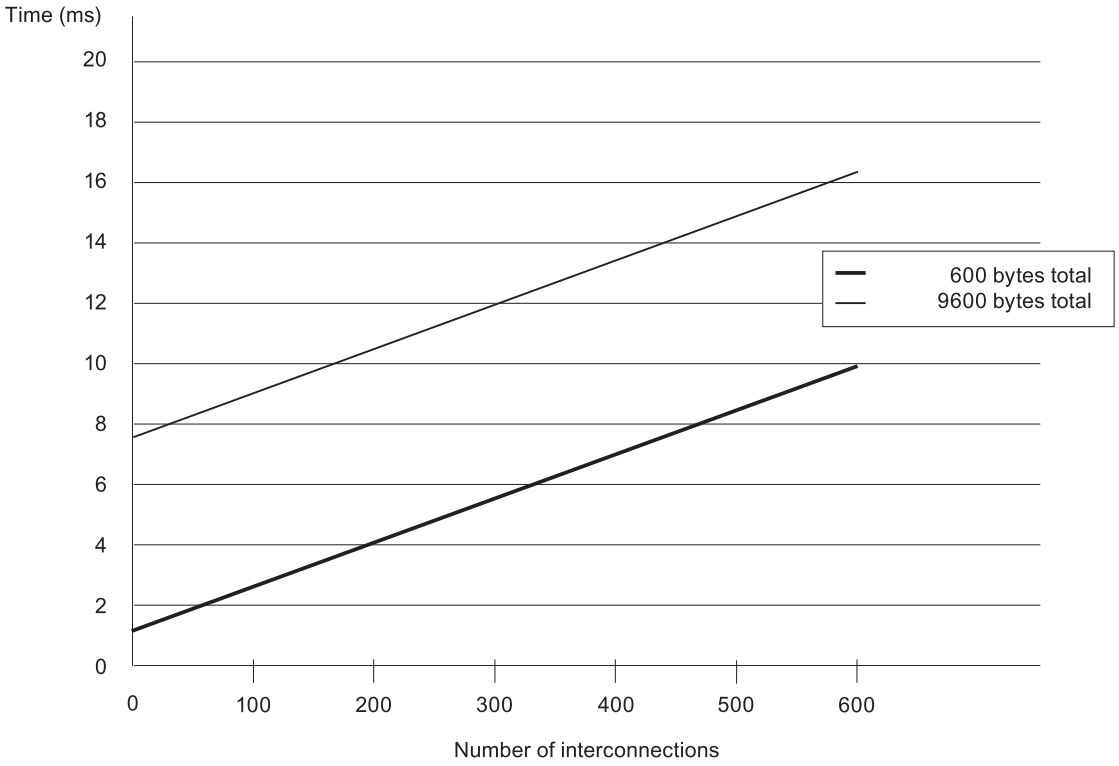


Figure 9-11 Processing time for sending and receiving

You can estimate the CBA response time using the information in this figure and the time you have set for the transmission frequency.

The following applies:

CBA response times =

Processing time on the transmitting CPU* +

Cycle time based on the configured transmission frequency** +

Processing time on the receiving CPU*

*) Add all input and output interconnections of the CPU to determine the processing time. You can read the processing time from the diagram based on the determined number of interconnections and amount of data on them.

**) The configured transmission frequency has a direct relationship to the actual cycle time in the network. For technical reasons, the cycle time is based on the square of the base cycle time of 1ms. The actual cycle time therefore corresponds to the next smaller square of the configure transmission frequency; the following relationships result from the specified values: (transmission frequency <-> cycle time): 1<->1 | 2<->2 | 5<->4 | 10<->8 | 20<->16 | 50<->32 | 100<->64 | 200<->128 | 500<->256 | 1000<->512

Note on the Processing Times for Cyclic Interconnections

- The processing times are based on 32 remote partners. Few remote partners reduces the processing times by approx. 0.02 ms per partner.
- The processing times are based on byte interconnections (single bytes or arrays).
- The processing times are applicable for situations in which the same transmission frequency is configured for all cyclic interconnections. Increased transmission frequency can improve the performance.
- When acyclic interconnections with the maximum amount of data are simultaneously active, the response times of the cyclic interconnections increase by approx. 33%.
- The example measurements were performed with a CPU 416-3 PN/DP. With a CPU 414-3 PN/DP the processing times increase by approx. 20%.

Response Time for Acyclic Interconnections

The resulting response time depends on the configured sampling frequency and the number of cyclic interconnections that are simultaneously active. You can see three examples for the resulting response times in the following table.

Table 9-11 Response time for acyclic interconnections

Configured sampling frequency	Resulting response time without cyclic interconnections	Resulting response time with cyclic interconnections (maximum amount of data)
200 ms	195 ms	700 ms
500 ms	480 ms	800 ms
1000 ms	950 ms	1050 ms

General Information about Achievable CBA Response Times

- The CBA response time increases if the CPU is performing additional tasks, such as programmed block communication or S7 connections.
- If you frequently call SFCs "PN_IN", "PN_OUT" or "PN_DP", you increase the CBA processing times and therefore increase CBA response time.
- A very small OB1 cycle increases the CBA response time when the PN interface is updated automatically (at the cycle control point).

Technical specifications

10

10.1 Technical Specification of the CPU 414-3 PN/DP; (6ES7414-3EM05-0AB0)

Data

CPU and firmware version	
Order no. [MLFB]	6ES7414-3EM05-0AB0
• Firmware version	V 5.0
Associated programming package	STEP 7 V 5.4 SP1 and higher
Memory	
Working memory	
• Integrated	1.4 MB for code 1.4 MB for data
Loading memory	
• Integrated	512 KB RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 MB
• Expandable RAM	With memory card (RAM) up to 64 MB
Backup with battery	Yes, all data
Typical processing times	
Processing times of	
• Bit operations	45 ns
• Word instructions	45 ns
• Fixed-point arithmetic	45 ns
• Floating-point arithmetic	135 ns
Timers/counters and their retentive address areas	
S7 counters	2048
• Retentive address areas, configurable	From C 0 to C 2047
• Preset	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes
• Type	SFB

CPU and firmware version	
S7 timers	2048
• Retentive address areas, configurable	From T 0 to T 2047
• Preset	No retentive timers
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB
Data areas and their retentive address areas	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Bit memory	8 KB
• Retentive address areas, configurable	From MB 0 to MB 8191
• Preset retentive address areas	MB 0 to MB 15
Clock flag bits	8 (1 flag byte)
Data blocks	Max. 6000 (DB 0 reserved) in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
Local data (can be set)	Max. 16 KB
• Preset	8 KB
Blocks	
OBs	See *Instruction List*
• Size	Max. 64 KB
Nesting depth	
• Per priority class	24
• Additionally within an error OB	1
FBs	Max. 3000 in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
FCs	Max. 3000 in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
Address areas (I/O)	
Total I/O address area	8 KB / 8 KB including diagnostics addresses for I/O interfaces, etc.
• Distributed	
MPI/DP interface	2 KB / 2 KB
DP interface	6 KB / 6 KB
PN interface	8 KB / 8 KB
Process image	8 KB / 8 KB (can be set)
• Preset	256 bytes / 256 bytes
• Number of process image partitions	Max. 15

CPU and firmware version	
• Consistent data	Max. 244 bytes

CPU and firmware version	
Digital channels	Max. 65536 / Max. 65536
• Centralized	Max. 65536 / Max. 65536
Analog channels	Max. 4096 / Max. 4096
• Centralized	Max. 4096 / Max. 4096
Removal	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended IM 467 cannot be used with the CP 443-1 EX4x in PN IO mode	
Number of PN controllers	
• Integrated	1
• Via CP 443-1 EX 41 in PN mode	Maximum 4 in central rack
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• PROFIBUS and Ethernet CPs including CP 443-5 Extended and IM 467	Max. 14
Time	
Real-time clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at – Power off – Power on	 Maximum deviation per day 1.7 s Maximum deviation per day 8.6 s
Operating hours counters	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes

CPU and firmware version	
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	As master or slave
• On Ethernet via NTP	Yes (as client)
S7 message functions	
Number of stations that can be used	
For block-specific messages (Alarm_S/SQ or Alarm_D/DQ)	31
For control-specific messages (ALARM_8 blocks, archive)	8
Symbol-related messages	Yes
• Number of messages – Total – 100 ms scheme – 500 ms scheme – 1000 ms scheme	 Max. 512 Max. 128 Max. 256 Max. 512
• Number of additional values per message – With 100 ms scheme – With 500 to 1000 ms scheme	 Max. 1 Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 100
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks and blocks for S7 communication (can be set)	Max. 600
• Preset	300
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	16
Test and startup functions	
Status/control variable	Yes
• Variable	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Forcing	Yes
• Variable	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 256
Block status	Yes
Single-step mode	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)

CPU and firmware version	
• Preset	120
Number of breakpoints	4

CPU and firmware version	
Communication	
PG/OP communication	Yes
Number of connectable OPs	31 with message processing Alarm S/SQ, Alarm D/DQ
Number of connection resources for S7 connections via all interfaces and CPs	32, with one each of those reserved for programming device and OP
Global data communication	Yes
• Number of GD circuits	Max. 8
• Number of GD packets – Transmitters – Receiving stations	 Max. 8 Max. 16
• Size of GD packets – Of which consistent	Max. 64 bytes 1 variable
S7 basic communication	Yes
• MPI Mode	Via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	Via SFC I_GET and I_PUT
• User data per job – Of which consistent	Max. 76 bytes 1 variable
S7 communication	Yes
• User data per job – Of which consistent	Max. 64 KB 1 variable (462 bytes)
S5-compatible communication	Via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job – Of which consistent	Max. 8 KB 240 bytes
Standard communication (FMS)	Yes (via CP and loadable FBs)
Web Server	Yes
Open IE communication via TCP/IP	
Number of connections / access points, total	max. 30
TCP/IP	Yes (via integrated PROFINET interface and loadable FBs)
• Maximum number of connections	30
• Data length, max.	32767 bytes
ISO on TCP	Yes (via integrated PROFINET interface or CP 443-1 EX41 and loadable FBs)
• Maximum number of connections	30
• Max. data length via integrated PROFINET interface	32767 bytes
• Max. data length via CP 443-1 EX41	1452 bytes
UDP	
• Maximum number of connections	30

CPU and firmware version	
• Data length, max.	1472 bytes

CPU and firmware version	
PROFINET CBA	
Reference setting for the CPU communication load	20%
Number of remote interconnecting partners	32
Number of master/slave functions	150
Total of all master/slave connections	4500
Data length of all incoming master/slave connections, max.	45000 bytes
Data length of all outgoing master/slave connections, max.	45000 bytes
Number of device-internal and PROFIBUS interconnections	1000
Data length of the device-internal and PROFIBUS interconnections, max.	16000 bytes
Data length per connection, max.	2000 bytes
Remote interconnections with acyclic transmission	
• Scan rate: Scan interval, min.	200 ms
• Number of incoming interconnections	250
• Number of outgoing interconnections	250
• Data length of all incoming interconnections, max.	8000 bytes
• Data length of all outgoing interconnections, max.	8000 bytes
• Data length per connection, (acyclic interconnections), max.	2000 bytes
Remote interconnections with cyclic transmission	
• Transmission frequency: Minimum transmission interval	1 ms
• Number of incoming interconnections	300
• Number of outgoing interconnections	300
• Data length of all incoming interconnections, max.	4800 bytes
• Data length of all outgoing interconnections	4800 bytes
• Data length per connection, (acyclic interconnections), max.	250 bytes
HMI variables via PROFINET (acyclic)	
• Update HMI variables	500 ms
• Number of stations that can be logged on for HMI variables (PN OPC/iMAP)	2*PN OPC / 1* iMAP
• Number of HMI variables	1000

CPU and firmware version	
• Data length of all HMI variables, max.	32000 bytes
PROFIBUS proxy functionality	
• supported	Yes
• Number of coupled PROFIBUS devices	32
• Data length per connection, max.	128 bytes (slave dependent)
Interfaces	
1st interface	
Type of interface	Integrated
Properties	RS 485/PROFIBUS
isolated	Yes
Power supply to interface 24 V rated voltage (15 to 30 V DC)	Maximum 150 mA
Number of connection resources	MPI: 32 DP: 16
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st interface MPI mode	
• Services – PG/OP communication – Routing – Global data communication – S7 basic communication – S7 communication – Time synchronization	 Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
1st interface DP master mode	
• Services – PG/OP communication – Routing – S7 basic communication – S7 communication – Constant Bus Cycle Time – SYNC/FREEZE – Enable/disable DP slaves – Time synchronization	 Yes Yes Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves	Max. 32
• Address area	Max. 2 KB inputs / 2 KB outputs

CPU and firmware version	
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 2 KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded.	

CPU and firmware version	
1st interface DP slave mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Services – Status/Control – Programming – Routing – Time synchronization	 Yes Yes Yes Yes
• DDBF file	http://www.ad.siemens.de/csi_e/gsd
• Transmission speed	Up to 12 Mbaud
• Transfer memory – Virtual slots – User data per address area – Of which consistent	244-byte inputs / 244-byte outputs Max. 32 Max. 32 bytes 32 bytes
2nd interface	
Type of interface	Integrated
Properties	Ethernet 2-port switch 2 x RJ45
Isolated	Yes
Autosensing (10/100 Mbaud)	Yes
Autonegation	Yes
Autocrossover	Yes
Functionality	
• PROFINET	Yes
Services	
• Programming device communication	Yes
• OP communication	Yes
• S7 communication – Max. configurable interconnections – Maximum number of instances	Yes 32, with one each of those reserved for programming device and OP 600
	Yes
• Routing	Yes
• PROFINET IO	Yes
• PROFINET CBA	Yes
Open IE communication	
• via TCP/IP	Yes
• ISO on TCP	Yes
• UDP	Yes
• Time synchronization	Yes

CPU and firmware version	
PROFINET IO	
PNO ID (hexadecimal)	813C
Number of integrated PROFINET IO controllers	1
Number of PROFINET IO devices that can be connected	256
Address area	max. 8 KB inputs/outputs
Number of submodules	Maximum 8192 Mixed modules have a factor of 2
Max. user data length including user data qualifiers	240 bytes per submodule
Max. user data consistency	240 bytes
Update Time	250 µs, 0.5 ms, 1 ms, 2 ms and 4 ms The minimum value is determined by the set communication portion for PROFINET IO, the number of IO devices and the amount of configured user data.
S7 protocol functions	
• Programming device functions	Yes
• OP functions	Yes
3rd. interface	
Type of interface	Plug-in interface module
Usable interface module	IF 964-DP
Properties	RS 485/PROFIBUS
isolated	Yes
Power supply to interface 24 V rated voltage (15 VDC to 30 VDC)	Maximum 150 mA
Number of connection resources	16
Functionality	
• PROFIBUS DP	DP master/DP slave
3rd interface DP master mode	
• Services – PG/OP communication – Routing – S7 basic communication – S7 communication – Constant bus cycle time – SYNC/FREEZE – Enable/disable DP slaves	 Yes Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves	Max. 96
• Address area	Max. 6 KB inputs / 6 KB outputs

CPU and firmware version	
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 6 KB inputs /6 KB outputs) accumulated by 96 slaves may not be exceeded	
3rd interface DP slave mode	
Specifications as for 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See *Instruction List*
Nesting levels	8
System functions (SFC)	See *Instruction List*
Number of SFCs active at the same time for every line	
• DPSYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	2
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1... 8
• DP_TOPOL	1
System function blocks (SFB)	See *Instruction List*
Number of SFBs active at the same time	
• RDREC	8
• WRREC	8
User program protection	Password security
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	80 µs

CPU and firmware version	
Isochronous mode	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following must apply: Number of bytes/100 + number of slaves < 26
Constant bus cycle time	Yes
Shortest clock pulse Longest clock pulse	1.0 ms 0.5 ms without use of SFC126, 127 32 ms
see *Isochronous Mode* manual	
Dimensions	
Mounting dimensions WxHxD (mm)	50x290x219
Slots required	2
Weight	approx. 0.9 kg
Voltages, currents	
Current consumption from the S7-400 bus (5 VDC)	Typical 1.2 A maximum 1.4 A
Current consumption from S7-400 bus (24 V DC) The CPU does not consume any current at 24 V, it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typical 125 µA maximum 300 µA
Maximum backup time	See *Module Specifications* reference manual, Section 3.3.
Incoming supply of external backup voltage to the CPU	5 to 15 V DC
Power loss	Typical 5.5 W

10.2 Technical Specification of the CPU 416-3 PN/DP; (6ES7416-3ER05-0AB0)

Data

CPU and firmware version	
Order no. [MLFB]	6ES7416-3ER05-0AB0
• Firmware version	V 5.0
Associated programming package	STEP 7 V 5.4 SP1 and higher
Memory	
Working memory	
• Integrated	5.6 MB for code 5.6 MB for data
Loading memory	
• Integrated	1024 KB RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 MB
• Expandable RAM	With memory card (RAM) up to 64 MB
Backup with battery	Yes, all data
Typical processing times	
Processing times of	
• Bit operations	30 ns
• Word instructions	30 ns
• Fixed-point arithmetic	30 ns
• Floating-point arithmetic	90 ns
Timers/counters and their retentive address areas	
S7 counters	2048
• Retentive address areas, configurable	From C 0 to C 2047
• Preset	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes
• Type	SFB
S7 timers	2048
• Retentive address areas, configurable	From T 0 to T 2047
• Preset	No retentive timers
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

CPU and firmware version	
Data areas and their retentive address areas	
Total retentive data area (including memory markers, timers, counters)	Total working and load memory (with backup battery)
Bit memory	16 KB
• Retentive address areas, configurable	MB 0 to MB 16383
• Preset retentive address areas	MB 0 to MB 15
Clock flag bits	8 (1 flag byte)
Data blocks	Max. 10000 (DB 0 reserved) in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
Local data (can be set)	Max. 32 KB
• Preset	16 KB
Blocks	
OBs	See *Instruction List*
• Size	Max. 64 KB
Nesting depth	
• Per priority class	24
• Additionally within an error OB	2
FBs	Max. 5000 in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
FCs	Max. 5000 in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
Address areas (I/O)	
Total I/O address area	16 KB / 16 KB including diagnostics addresses for I/O interfaces, etc.
• Distributed	
MPI/DP interface	2 KB / 2 KB
DP interface	8 KB / 8 KB
PN interface	8 KB / 8 KB
Process image	16 KB / 16 KB (can be set)
• Preset	512 bytes / 512 bytes
• Number of process image partitions	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 131072 / Max. 131072
• Centralized	Max. 131072 / Max. 131072
Analog channels	Max. 8192 / Max. 8192
• Centralized	Max. 8192 / Max. 8192

CPU and firmware version	
Extension	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended IM 467 cannot be used with the CP 443-1 EX4x in PN IO mode	
Number of PN controllers	
• Integrated	1
• Via CP 443-1 EX 41 in PN mode	Maximum 4 in central rack
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• PROFIBUS and Ethernet CPs including CP 443-5 Extended and IM 467	Max. 14
Time	
Real-time clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at – Power off – Power on	 Maximum deviation per day 1.7 s Maximum deviation per day 8.6 s
Operating hours counters	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	As master or slave
• On Ethernet via NTP	Yes (as client)

CPU and firmware version	
S7 message functions	
Number of stations that can be used	
For block-specific messages (Alarm_S/SQ or Alarm_D/DQ)	63
For control-specific messages (ALARM_8 blocks, archive)	8
Symbol-related messages	Yes
• Number of messages – Total – 100 ms scheme – 500 ms scheme – 1000 ms scheme	 Max. 1024 Max. 128 Max. 512 Max. 1024
• Number of additional values per message – With 100 ms scheme – With 500, 1000 ms scheme	 Max. 1 Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 200
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks and blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32
Test and startup functions	
Status/control variables	Yes
• Variable	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of tags	Max. 70
Forcing	Yes
• Variable	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of tags	Max. 512
Block status	Yes
Single-step mode	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

CPU and firmware version	
Communication	
PG/OP communication	Yes
Number of connectable OPs	63 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for programming device and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packets – Transmitters – Receiving stations	 Max. 16 Max. 32
• Size of GD packets – Of which consistent	Max. 64 bytes 1 variable
S7 basic communication	Yes
• MPI Mode	Via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	Via SFC I_GET and I_PUT
• User data per job – Of which consistent	Max. 76 bytes 1 variable
S7 communication	Yes
• User data per job – Of which consistent	Max. 64 KB 1 variable (462 bytes)
S5-compatible communication	Via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job – Of which consistent	Max. 8 KB 240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Web Server	Yes
Open IE communication via TCP/IP	
Number of connections / access points, total	max. 30
TCP/IP	Yes (via integrated PROFINET interface and loadable FBs)
• Maximum number of connections	30
• Data length, max.	32767 bytes
ISO on TCP	Yes (via integrated PROFINET interface or CP 443-1 EX 41 and loadable FBs)
• Maximum number of connections	30
• Max. data length via integrated PROFINET interface	32767 bytes
• Max. data length via CP 443-1 EX41	1452 bytes
UDP	
• Maximum number of connections	30
• Data length, max.	1472 bytes

CPU and firmware version	
PROFINET CBA	
Reference setting for the CPU communication load	20%
Number of remote interconnecting partners	32
Number of master/slave functions	150
Total of all master/slave connections	6000
Data length of all incoming master/slave connections, max.	65000 bytes
Data length of all outgoing master/slave connections, max.	65000 bytes
Number of device-internal and PROFIBUS interconnections	1000
Data length of the device-internal and PROFIBUS interconnections, max.	16000 bytes
Data length per connection, max.	2000 bytes
Remote interconnections with acyclic transmission	
• Scan rate: Scan interval, min.	200 ms
• Number of incoming interconnections	500
• Number of outgoing interconnections	500
• Data length of all incoming interconnections, max.	1600 bytes
• Data length of all outgoing interconnections, max.	1600 bytes
• Data length per connection, (acyclic interconnections), max.	2000 bytes
Remote interconnections with cyclic transmission	
• Transmission frequency: Minimum transmission interval	1 ms
• Number of incoming interconnections	300
• Number of outgoing interconnections	300
• Data length of all incoming interconnections, max.	4800 bytes
• Data length of all outgoing interconnections	4800 bytes
• Data length per connection, (acyclic interconnections), max.	250 bytes
HMI variables via PROFINET (acyclic)	
• Update HMI variables	500 ms
• Number of stations that can be logged on for HMI variables (PN OPC/iMAP)	2*PN OPC / 1* iMAP
• Number of HMI variables	1000

CPU and firmware version	
• Data length of all HMI variables, max.	32000 bytes
PROFIBUS proxy functionality	
• supported	Yes
• Number of coupled PROFIBUS devices	32
• Data length per connection, max.	128 bytes (slave dependent)
Interfaces	
1st interface	
Type of interface	Integrated
Properties	RS 485/PROFIBUS
isolated	Yes
Power supply to interface 24 V rated voltage (15 to 30 VDC)	Maximum 150 mA
Number of connection resources	MPI: 44 DP: 32 a diagnostic repeater in the line reduces the number of connection resources on the line by 1
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st interface MPI mode	
• Services – PG/OP communication – Routing – Global data communication – S7 basic communication – S7 communication – Time synchronization	 Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
1st interface DP master mode	
• Services – PG/OP communication – Routing – S7 basic communication – S7 communication – Constant Bus Cycle Time – SYNC/FREEZE – Enable/disable DP slaves – Time synchronization	 Yes Yes Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves	Max. 32
• Address area	Max. 2 KB inputs / 2 KB outputs

CPU and firmware version	
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 2 KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st interface DP slave mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Services – Status/Control – Programming – Routing – Time synchronization	 Yes Yes Yes Yes
• DDBF file	http://www.ad.siemens.de/csi_e/gsd
• Transmission speed	Up to 12 Mbaud
• Transfer memory – Virtual slots – User data per address area – Of which consistent	244-byte inputs / 244-byte outputs Max. 32 Max. 32 bytes 32 bytes
2nd interface	
Type of interface	Integrated
Properties	Ethernet 2-port switch 2 x RJ45
Isolated	Yes
Autosensing (10/100 Mbaud)	Yes
Autonegation	Yes
Autocrossover	Yes
Functionality	
• PROFINET	Yes
Services	
• Programming device communication	Yes
• OP communication	Yes
• S7 communication – Max. configurable interconnections – Maximum number of instances	Yes 32, with one each of those reserved for programming device and OP 600
	Yes
• Routing	Yes
• PROFINET IO	Yes
• PROFINET CBA	Yes

CPU and firmware version	
Open IE communication	
• via TCP/IP	Yes
• ISO on TCP	Yes
• UDP	Yes
• Time synchronization	Yes

CPU and firmware version	
PROFINET IO	
PNO ID (hexadecimal)	813D
Number of PROFINET IO devices that can be connected	256
Address area	max. 8 KB inputs/outputs
Number of submodules	Maximum 8192 Mixed modules have a factor of 2
Max. user data length including user data qualifiers	240 bytes per submodule
Max. user data consistency	240 bytes
Update Time	250 µs, 0.5 ms, 1 ms, 2 ms and 4 ms The minimum value is determined by the set communication portion for PROFINET IO, the number of IO devices and the amount of configured user data.
S7 protocol functions	
• Programming device functions	Yes
• OP functions	Yes
3rd. interface	
Type of interface	Plug-in interface module
Usable interface module	IF 964-DP
Properties	RS 485/PROFIBUS
isolated	Yes
Power supply to interface 24 V rated voltage (15 to 30 VDC)	Maximum 150 mA
Number of connection resources	32, a diagnostic repeater in the line reduces the number of connection resources on the line by 1
Functionality	
• PROFIBUS DP	DP master/DP slave
3rd interface DP master mode	
• Services – PG/OP communication – Routing – S7 basic communication – S7 communication – Constant Bus Cycle Time – SYNC/FREEZE – Enable/disable DP slaves	 Yes Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves	Max. 125
• Address area	Max. 8 KB inputs / 8 KB outputs
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes

CPU and firmware version	
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 8 KB inputs /8 KB outputs) accumulated by 125 slaves may not be exceeded	
3rd interface DP slave mode	
Specifications as for 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See *Instruction List*
Nesting levels	8
System functions (SFC)	See *Instruction List*
Number of SFCs active at the same time for every line	
• DPSYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	2
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1... 8
• DP_TOPOL	1
System function blocks (SFB)	See *Instruction List*
Number of SFBs active at the same time	
• RDREC	8
• WRREC	8
User program protection	Password security
Access to consistent data in the process image	Yes
CiR synchronization time	
Base Load	100 ms
Time per I/O byte	40 µs
Isochronous mode	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following must apply: Number of bytes/100 + number of slaves < 40
Constant Bus Cycle Time	Yes
Shortest clock pulse Longest clock pulse	1 ms 0.5 ms without use of SFC126, 127 32 ms
see *Isochronous Mode* manual	

CPU and firmware version	
Dimensions	
Mounting dimensions WxHxD (mm)	50x290x219
Slots required	2
Weight	Approx. 0.9 kg
Voltages, currents	
Current consumption from the S7-400 bus (5 VDC)	Typical 1.2 A maximum 1.4 A
Current consumption from S7-400 bus (24 V DC) The CPU does not consume any current at 24 V, it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typical 125 µA maximum 300 µA
Maximum backup time	See *Module Specifications* reference manual, Section 3.3.
Incoming supply of external backup voltage to the CPU	5 to 15 V DC
Power loss	Typical 5.5 W

10.3 Technical Specification of the CPU 416-3F PN/DP; (6ES7416-3FR05-0AB0)

Data

CPU and firmware version	
Order no. [MLFB]	6ES7416-3FR05-0AB0
• Firmware version	V 5.0
Associated programming package	STEP 7 V 5.4 SP1 and higher
Memory	
Working memory	
• Integrated	5.6 MB for code 5.6 MB for data
Loading memory	
• Integrated	1024 KB RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 MB
• Expandable RAM	With memory card (RAM) up to 64 MB
Backup with battery	Yes, all data
Typical processing times	
Processing times of	
• Bit operations	30 ns
• Word instructions	30 ns
• Fixed-point arithmetic	30 ns
• Floating-point arithmetic	90 ns
Timers/counters and their retentive address areas	
S7 counters	2048
• Retentive address areas, configurable	From C 0 to C 2047
• Preset	From C 0 to C 7
• Counting range	0 to 999
IEC counters	Yes
• Type	SFB
S7 timers	2048
• Retentive address areas, configurable	From T 0 to T 2047
• Preset	No retentive timers
• Timer range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

CPU and firmware version	
Data areas and their retentive address areas	
Total retentive data area (including memory markers, timers, counters)	Total working and load memory (with backup battery)
Bit memory	16 KB
• Retentive address areas, configurable	MB 0 to MB 16383
• Preset retentive address areas	MB 0 to MB 15
Clock flag bits	8 (1 flag byte)
Data blocks	Max. 10000 (DB 0 reserved) in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
Local data (can be set)	Max. 32 KB
• Preset	16 KB
Blocks	
OBs	See *Instruction List*
• Size	Max. 64 KB
Nesting depth	
• Per priority class	24
• Additionally within an error OB	2
FBs	Max. 5000 in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
FCs	Max. 5000 in the 1 to 16 000 range of numbers
• Size	Max. 64 KB
Address areas (I/O)	
Total I/O address area	16 KB / 16 KB including diagnostics addresses for I/O interfaces, etc.
• Distributed	
MPI/DP interface	2 KB / 2 KB
DP interface	8 KB / 8 KB
PN interface	8 KB / 8 KB
Process image	16 KB / 16 KB (can be set)
• Preset	512 bytes / 512 bytes
• Number of process image partitions	Max. 15
• Consistent data	Max. 244 bytes
Digital channels	Max. 131072 / Max. 131072
• Centralized	Max. 131072 / Max. 131072
Analog channels	Max. 8192 / Max. 8192
• Centralized	Max. 8192 / Max. 8192

CPU and firmware version	
Removal	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IF 964-DP	1
• Via IM 467	Max. 4
• Via CP 443-5 Extended	Max. 10
IM 467 cannot be used with the CP 443-5 Extended IM 467 cannot be used with the CP 443-1 EX4x in PN IO mode	
Number of PN controllers	
• Integrated	1
• Via CP 443-1 EX 41 in PN mode	Maximum 4 in central rack
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• PROFIBUS and Ethernet CPs including CP 443-5 Extended and IM 467	Max. 14
Time	
Real-time clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at – Power off – Power on	 Maximum deviation per day 1.7 s Maximum deviation per day 8.6 s
Operating hours counters	8
• Number	0 to 7
• Value range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI, DP and IF 964 DP	As master or slave
• On Ethernet via NTP	Yes (as client)

CPU and firmware version	
S7 message functions	
Number of stations that can be used	
For block-specific messages (Alarm_S/SQ or Alarm_D/DQ)	63
For control-specific messages (ALARM_8 blocks, archive)	8
Symbol-related messages	Yes
• Number of messages – Total – 100 ms scheme – 500 ms scheme – 1000 ms scheme	 Max. 1024 Max. 128 Max. 512 Max. 1024
• Number of additional values per message – With 100 ms scheme – With 500, 1000 ms scheme	 Max. 1 Max. 10
Block-related messages	Yes
• Simultaneously active ALARM_S/SQ blocks and ALARM_D/DQ blocks	Max. 200
ALARM_8 blocks	Yes
• Number of communication jobs for ALARM_8 blocks and blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32
Test and startup functions	
Status/control variables	Yes
• Variable	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of tags	Max. 70
Forcing	Yes
• Variable	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of tags	Max. 512
Block status	Yes
Single-step mode	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

CPU and firmware version	
Communication	
PG/OP communication	Yes
Number of connectable OPs	63 with message processing
Number of connection resources for S7 connections via all interfaces and CPs	64, with one each of those reserved for programming device and OP
Global data communication	Yes
• Number of GD circuits	Max. 16
• Number of GD packets – Transmitters – Receiving stations	 Max. 16 Max. 32
• Size of GD packets – Of which consistent	Max. 64 bytes 1 variable
S7 basic communication	Yes
• MPI Mode	Via SFC X_SEND, X_RCV, X_GET and X_PUT
• DP Master Mode	Via SFC I_GET and I_PUT
• User data per job – Of which consistent	Max. 76 bytes 1 variable
S7 communication	Yes
• User data per job – Of which consistent	Max. 64 KB 1 variable (462 bytes)
S5-compatible communication	Via FC AG_SEND and AG_RECV, max. via 10 CP 443-1 or 443-5)
• User data per job – Of which consistent	Max. 8 KB 240 bytes
Standard communication (FMS)	Yes (via CP and loadable FB)
Web Server	Yes
Open IE communication via TCP/IP	
Number of connections / access points, total	max. 30
TCP/IP	Yes (via integrated PROFINET interface and loadable FBs)
• Maximum number of connections	30
• Data length, max.	32767 bytes
ISO on TCP	Yes (via integrated PROFINET interface or CP 443-1 EX 41 and loadable FBs)
• Maximum number of connections	30
• Max. data length via integrated PROFINET interface	32767 bytes
• Max. data length via CP 443-1 EX 41	1452 bytes
UDP	
• Maximum number of connections	30
• Data length, max.	1472 bytes

CPU and firmware version	
PROFINET CBA	
Reference setting for the CPU communication load	20%
Number of remote interconnecting partners	32
Number of master/slave functions	150
Total of all master/slave connections	6000
Data length of all incoming master/slave connections, max.	65000 bytes
Data length of all outgoing master/slave connections, max.	65000 bytes
Number of device-internal and PROFIBUS interconnections	1000
Data length of the device-internal and PROFIBUS interconnections, max.	16000 bytes
Data length per connection, max.	2000 bytes
Remote interconnections with acyclic transmission	
• Scan rate: Scan interval, min.	200 ms
• Number of incoming interconnections	500
• Number of outgoing interconnections	500
• Data length of all incoming interconnections, max.	16000 bytes
• Data length of all outgoing interconnections, max.	16000 bytes
• Data length per connection, (acyclic interconnections), max.	1400 bytes
Remote interconnections with cyclic transmission	
• Transmission frequency: Minimum transmission interval	1 ms
• Number of incoming interconnections	300
• Number of outgoing interconnections	300
• Data length of all incoming interconnections, max.	4800 bytes
• Data length of all outgoing interconnections	4800 bytes
• Data length per connection, (acyclic interconnections), max.	250 bytes
HMI variables via PROFINET (acyclic)	
• Update HMI variables	500 ms
• Number of stations that can be logged on for HMI variables (PN OPC/iMAP)	2*PN OPC / 1* iMAP
• Number of HMI variables	1000

CPU and firmware version	
• Data length of all HMI variables, max.	32000 bytes
PROFIBUS proxy functionality	
• supported	Yes
• Number of coupled PROFIBUS devices	32
• Data length per connection, max.	128 bytes (slave dependent)
Interfaces	
1st interface	
Type of interface	Integrated
Properties	RS 485/PROFIBUS
isolated	Yes
Power supply to interface 24 V rated voltage (15 to 30 VDC)	Maximum 150 mA
Number of connection resources	MPI: 44 DP: 32 a diagnostic repeater in the line reduces the number of connection resources on the line by 1
Functionality	
• MPI	Yes
• PROFIBUS DP	DP master/DP slave
1st interface MPI mode	
• Services – PG/OP communication – Routing – Global data communication – S7 basic communication – S7 communication – Time synchronization	 Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
1st interface DP master mode	
• Services – PG/OP communication – Routing – S7 basic communication – S7 communication – Constant Bus Cycle Time – SYNC/FREEZE – Enable/disable DP slaves – Time synchronization	 Yes Yes Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves	Max. 32
• Address area	Max. 2 KB inputs / 2 KB outputs

CPU and firmware version	
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 2 KB inputs /2 KB outputs) accumulated by 32 slaves may not be exceeded	
1st interface DP slave mode	
You can only configure the CPU once as a DP slave even if the CPU has several interfaces.	
• Services – Status/Control – Programming – Routing – Time synchronization	 Yes Yes Yes Yes
• DDBF file	http://www.ad.siemens.de/csi_e/gsd
• Transmission speed	Up to 12 Mbaud
• Transfer memory – Virtual slots – User data per address area – Of which consistent	244-byte inputs / 244-byte outputs Max. 32 Max. 32 bytes 32 bytes
2nd interface	
Type of interface	Integrated
Properties	Ethernet 2-port switch 2 x RJ45
Isolated	Yes
Autosensing (10/100 Mbaud)	Yes
Autonegation	Yes
Autocrossover	Yes
Functionality	
• PROFINET	Yes
Services	
• Programming device communication	Yes
• OP communication	Yes
• S7 communication – Max. configurable interconnections – Maximum number of instances	Yes 32, with one each of those reserved for programming device and OP 600
	Yes
• Routing	Yes
• PROFINET IO	Yes
• PROFINET CBA	Yes

CPU and firmware version	
Open IE communication	
• via TCP/IP	Yes
• ISO on TCP	Yes
• UDP	Yes
• Time synchronization	Yes

CPU and firmware version	
PROFINET IO	
PNO ID (hexadecimal)	813E
Number of integrated PROFINET IO controllers	1
Number of PROFINET IO devices that can be connected	256
Address area	max. 8 KB inputs/outputs
Number of submodules	Maximum 8192 Mixed modules have a factor of 2
Max. user data length including user data qualifiers	240 bytes per submodule
Max. user data consistency	240 bytes
Update Time	250 µs, 0.5 ms, 1 ms, 2 ms and 4 ms The minimum value is determined by the set communication portion for PROFINET IO, the number of IO devices and the amount of configured user data.
S7 protocol functions	
• Programming device functions	Yes
• OP functions	Yes
3rd. interface	
Type of interface	Plug-in interface module
Usable interface module	IF 964-DP
Properties	RS 485/PROFIBUS
isolated	Yes
Power supply to interface 24 V rated voltage (15 to 30 VDC)	Maximum 150 mA
Number of connection resources	32, a diagnostic repeater in the line reduces the number of connection resources on the line by 1
Functionality	
• PROFIBUS DP	DP master/DP slave
3rd interface DP master mode	
• Services – PG/OP communication – Routing – S7 basic communication – S7 communication – Constant Bus Cycle Time – SYNC/FREEZE – Enable/disable DP slaves	 Yes Yes Yes Yes Yes Yes Yes
• Transmission rates	Up to 12 Mbaud
• Number of DP slaves	Max. 125
• Address area	Max. 8 KB inputs / 8 KB outputs

CPU and firmware version	
• User data per DP slave	Max. 244 bytes inputs, max.244 bytes outputs, max. 244 slots each with max. 128 bytes
Note: • The accumulated number of input bytes at the slots may not exceed 244 • The accumulated number of output bytes at the slots may not exceed 244 • The maximum address area of the interface (max. 8 KB inputs /8 KB outputs) accumulated by 125 slaves may not be exceeded	
3rd interface DP slave mode	
Specifications as for 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See *Instruction List*
Nesting levels	8
System functions (SFC)	See *Instruction List*
Number of SFCs active at the same time for every line	
• DPSYC_FR	2
• D_ACT_DP	4
• RD_REC	8
• WR_REC	8
• WR_PARM	8
• PARM_MOD	2
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1... 8
• DP_TOPOL	1
System function blocks (SFB)	See *Instruction List*
Number of SFBs active at the same time	
• RDREC	8
• WRREC	8
User program protection	Password security
Access to consistent data in the process image	Yes
CiR synchronization time	
Base Load	100 ms
Time per I/O byte	40 µs

CPU and firmware version	
Isochronous mode	
User data per clock synchronous slave	Max. 244 bytes
Maximum number of bytes and slaves in a process image partition	The following must apply: Number of bytes/100 + number of slaves < 40
Constant Bus Cycle Time	Yes
Shortest clock pulse Longest clock pulse	1 ms 0.5 ms without use of SFC126, 127 32 ms
see *Isochronous Mode* manual	
Dimensions	
Mounting dimensions WxHxD (mm)	50x290x219
Slots required	2
Weight	Approx. 0.9 kg
Voltages, currents	
Current consumption from the S7-400 bus (5 VDC)	Typical 1.2 A maximum 1.4 A
Current consumption from S7-400 bus (24 V DC) The CPU does not consume any current at 24 V, it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typical 125 µA maximum 300 µA
Maximum backup time	See *Module Specifications* reference manual, Section 3.3.
Incoming supply of external backup voltage to the CPU	5 to 15 V DC
Power loss	Typical 5.5 W

10.4 Technical specifications of the memory cards

Data

Name	Order No.	Current consumption at 5 V	Backup currents
MC 952 / 64 Kbytes / RAM	6ES7952-0AF00-0AA0	typ. 20 mA Max. 50 mA	Typical 0.5 µA Max. 20 µA
MC 952 / 256 Kbytes / RAM	6ES7952-1AH00-0AA0	Typical 35 mA Max. 80 mA	Typical 1 µA Max. 40 µA
MC 952 / 1 MB / RAM	6ES7952-1AK00-0AA0	Typical 40 mA 90 mA max.	Typical 3 µA Max. 50 µA
MC 952 / 2 MB / RAM	6ES7952-1AL00-0AA0	Typical 45 mA 100 mA max.	Typical 5 µA Max. 60 µA
MC 952 / 4 MB / RAM	6ES7952-1AM00-0AA0	Typical 45 mA 100 mA max.	Typical 5 µA Max. 60 µA
MC 952 / 8 MB / RAM	6ES7952-1AP00-0AA0	Typical 45 mA 100 mA max.	Typical 5 µA Max. 60 µA
MC 952 / 16 MB / RAM	6ES7952-1AS00-0AA0	Typical 100 mA 150 mA max.	Typical 50 µA Max. 125 µA
MC 952 / 64 MB / RAM	6ES7952-1AY00-0AA0	Typical 100 mA 150 mA max.	Typical 100 µA Max. 500 µA
MC 952 / 64 KB / 5V FLASH	6ES7952-0KF00-0AA0	Typical 15 mA Max. 35 mA	–
MC 952 / 256 KB / 5V FLASH	6ES7952-0KH00-0AA0	Typical 20 mA Max. 45 mA	–
MC 952 / 1 Mbytes / 5V Flash	6ES7952-1KK00-0AA0	Typical 40 mA Max. 90 mA	–
MC 952 / 2 Mbytes / 5V Flash	6ES7952-1KL00-0AA0	Typical 50 mA Max. 100 mA	–
MC 952 / 4 Mbytes / 5V Flash	6ES7952-1KM00-0AA0	Typical 40 mA Max. 90 mA	–
MC 952 / 8 Mbytes / 5V Flash	6ES7952-1KP00-0AA0	Typical 50 mA Max. 100 mA	–
MC 952 / 16 Mbytes / 5V Flash	6ES7952-1KS00-0AA0	Typical 55 mA Max. 110 mA	–
MC 952 / 32 Mbytes / 5V Flash	6ES7952-1KT00-0AA0	Typical 55 mA Max. 110 mA	–
MC 952 / 64 Mbytes / 5V Flash	6ES7952-1KY00-0AA0	Typical 55 mA Max. 110 mA	–
Dimensions WxHxD (in mm)		7.5 x 57 x 87	
Weight		Max. 35 g	
EMC protection		Provided by construction	

IF 964-DP interface module

11

11.1 Using the IF 964-DP interface module

Order numbers

You can use the IF 964-DP interface module with order number 6ES7964-2AA04-0AB0 in the CPUs of the S7-400 as of firmware version 4.0.

The interface module identifier is on the front panel and can therefore be identified when it is installed.

Features

The IF 964-DP is used to connect distributed I/Os over "PROFIBUS-DP". The module has a floating RS-485 interface. The transmission rate is 12 Mbps maximum.

The permitted cable length depends on the transmission rate and the number of nodes. On a point-to-point link at a transmission rate of 12 Mbps, a cable length of 100 m is possible and at 9.6 Kbps, a length of 1200 m can be achieved.

The system can be expanded up to 125 stations.

Figure 11-1 IF 964-DP interface module

Note

The IF 964-DP may only be removed or inserted when the power is turned off.

If you remove the interface module when the power is turned on, the CPU changes to the DEFECT mode.

Further information

You will find information on "PROFIBUS-DP" in the following brochures and manuals:

- Manuals on the DP masters, for example *programmable logic controller S7-300* or *automation system S7-400* for the PROFIBUS-DP interface
- Manuals on the DP slaves, for example, *distributed I/O station ET 200M* or *distributed I/O station ET 200C*
- Manuals on *STEP 7*

11.2 Pin assignment of the IF 964-DP interface module

Connector X1

There is a 9-pin D-sub female connector on the front panel of the module for connecting the cable. You can see the pin assignment in the following table.

Table 11-1 Female connector IF1 IF 964-DP (9-pin D-sub)

Pin	Signal	Meaning	Direction
1	–		
2	M 24	24 V reference potential (6ES7964-2AA01-0AB0)	Output
3	LTG_B	Line B	Input/Output
4	RTSAS	request to send (AS)	Output
5	$M5_{ext}$	Functional ground (isolated)	Output
6	$P5_{ext}$	+ 5 V (floating), max. 920 mA (to supply the bus terminator)	Output
7	P 24 V	+24 V, max. 150 mA, non-floating	Output
8	LTG_A	Line A	Input
9	–		

11.3 Technical specifications

Technical specifications

The IF 964-DP interface module obtains its power from the CPU. The technical specifications include the necessary current consumption to allow dimensioning of the power supply unit.

Dimensions and weight	
Dimensions W x H x D (mm)	26 x 54 x 130
Weight	0.065 kg
Performance features	
Transmission rate	9.6 Kbps to 12 Mbps
Length of cable • at 9.6 Kbps • at 12 Mbps	 maximum 1200 m maximum 100 m
Number of stations	≤125 (depending on the CPU used)
Physical interface characteristics	RS-485
Isolation	Yes
Voltages, Currents	
Power supply	supplied by the S7-400
Current consumption from the S7-400 bus The CPU does not consume any current at 24 V, it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the DP interface, however maximum of 150 mA
Possible load of the floating 5 V ($P5_{ext}$)	Maximum 90 mA
Possible load of the 24 V	Maximum 150 mA
Module identifier	C_H
Power loss	1 W

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